Brief Summary of L1 Simulation Upgrade

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BaBar Collaboration Meeting
SLAC

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First production code contributed!

Release 14.3.0 and greater

- L1DctData
- modified L1DTsfDigi, new L1DZpdDigi
- L1DctOnline

Abstract interface for TSF LUT

All interfaces with “outside world”

~ 20 packages in total
i.e. L1TFMon, L3, OepSequences, ...

Remaining L1Sim changes are (mostly) inside the “black box”

Online Build not needed? (yet...)
This IS the current SP6 (14.3.X)

Base simulation code unchanged,
only the interface elements (Digis, TsfLUT)
Significant upgrade to L1 Simulation

Could be deployed in SP6 to improve simulation of Run4 data

Time estimate?? (~2 months)
Full L1Sim upgrade needed for hardware change

In principle can be ready shortly after Phase I completed (and validated)

Real work needed in TrigConfig (best to leave to überexperte)
Real concerns for how to validate (old) simulation code/boards

Possible Options

- Teststand
- Real Data
- trgDC comparison
- Data-MC comparison

Each has advantages/disadvantages

Probably no single one is sufficient

Real work to be done here...
Teststand Validation

Simulation

Board In

BoardSim

Board Out

Teststand

Input Mem

Hardware

Output Mem

• Load arbitrary or simulated bit patterns into board memories
• Compare with simulation expectation

Advantages

Bit-level comparison

Disadvantages

Cumbersome, need good input patterns, hard to test “system” problems

Possible to extend to multi-board?
Real Data Validation

- Use real data taken in IR2
- Compare hardware result with simulation

Advantages

Proper event mix
Could be run continuously (trickle stream)

Disadvantages

Bit-level not possible
Meaningful comparisons not obvious
• Start with DchDigis (real or simulated)
• Compare parallel simulation output

Advantages

Straightforward to implement
Tests “whole system”

Disadvantages

Don’t necessarily want agreement!
Not a direct validation of the hardware

(The plan is to actually improve something...)
• Start with real data (XTC file)
• Compare high-level “physics” output

Advantages

Straightforward to implement
Tests “whole system”
Test quantities that really matter?

Disadvantages

Limited comparisons available (L1A)
Will not find all problems
Will never find rare/subtle differences
Simulation Tools

Moose

- Ultimately where we want this to run...
- Add new modules to `L1SimL1TrigSequence`

This works, although is cumbersome for detailed debugging

Bogus/SimApp model

- Matthias Steinke working on “Kangerized” versions
- Can then generate Bogus data and repeatedly run simulation (as before)

Need to define `L1DctDataK`

Teststand convertor

- Translate simulated data into memory maps
- Works for TSF, possibly ZPD?

Needs work for multi-board
Is this really useful?
Well past time to get this finished!

Simulation can still beat hardware
(4 years too late for Runs 1-3...)