Discussion items for luminosity measurements at the ILC

David Strom – University of Oregon

- My suggestions are based on my experience with the LEP I OPAL luminosity measurement:

  ⇒ This was an enormous effort based on work of scores of people between (1990 conception) to 2000 (final publication)


  ⇒ Most recent result (measurement of $\alpha_{QED}$) running just accepted for publication

  CERN-EP-2005-024
• Impossible to measure luminosity

\[ \frac{1}{\theta^3} \]

distribution without small radial bias and very good resolution

⇒ Best to measure position of the electromagnetic shower rather than electron track

⇒ Since the radial measurement must be very well understood arrange other cuts to remove only a few events
- Example electromagnetic spectrum with and without acollinearity cut

OPAL
• Use very tight acollinearity cut for energy tune-up

OPAL

![Graphs showing energy distribution for OPAL experiment]

Snowmass 05
4
23 August 05 – David Strom – UO
• Make detector uniform so that no fiducial cuts in $\phi$ etc will be needed.

• What will the background from off-momentum beam particles be? Depends on vacuum near the interaction region.

  ⇒ Don’t make the pads too big in either radius or phi, need to separate background clusters from real Bhabhas.

• Background from low momentum pairs will probably be more important

  ⇒ Detector must be able to measure "min-bias" shape of background on a bunch-by-bunch basis
Detector Geometry

- It is essential to survey the detector at the micron level with cosmic ray muons or test beam.
  ⇒ Electronics must have MIP sensitivity even if it is not needed by the luminosity measurement
  ⇒ MIP sensitivity needed for possible muon veto (See Graham Wilson’s Calorimeter talk).

- Detectors should fit on a single wafer

- SiD geometry
  \[ R_{min} \approx 8.7 \text{ cm (}\sim 50\text{mrad)} \]
  \[ R_{max} \approx 24.7 \text{ cm (}\sim 150\text{mrad)} \]
  ⇒ 8 inch wafers would be needed

- Rate at 500 GeV is \sim 8 \text{ bhabhas bunch train} – Inner radius could be much larger and 6 inch wafers used
Is this segmentation reasonable?

- Assume 20 layers, 1 $X_0$ and 2 $X_0$

- Assume two readout chips/wafer (128 channels/chip)
  
  \[ 2 \times 16 \times 20 \times 2 = 1280 \text{ electronics chips} \]

- Assume Successive Approximation ADC with 12 bits + range, digitizing at 3MHz (internal clock is 36MHz). Data rate is 576 MBytes/s/chip during bunch train ($\sim 3.0$MBytes/s sustained)

- On board electronics cost will be dominated by development costs (very similar to run needed for test beam)

- Won’t save much money by reducing channels/wafer

- Power consumption should be reasonable, but no design yet for cooling in the endcap in SiD. LDC will be easier.
• Biggest unsolved problem: How to avoid gaps in end cap/lum cal coverage

• Good but impossible to open

• Has dead area between LAT and endcap