
Time and signal processing using solid state detectors

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- Introduction
- Semiconductor detector characteristics
- Electronics limitations
- Expectation for trackers
- Lab studies (Calorimeters)
- Toy Monte Carlo studies (Calorimeters)

Much of this work was carried with the help of the Si-W calorimeter group*:

Si-W work – personnel and responsibilities

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Electronics,
Mechanical Design,
Simulation

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Si Detectors,
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Simulation

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Electronics

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* *mistakes and errors are mine*

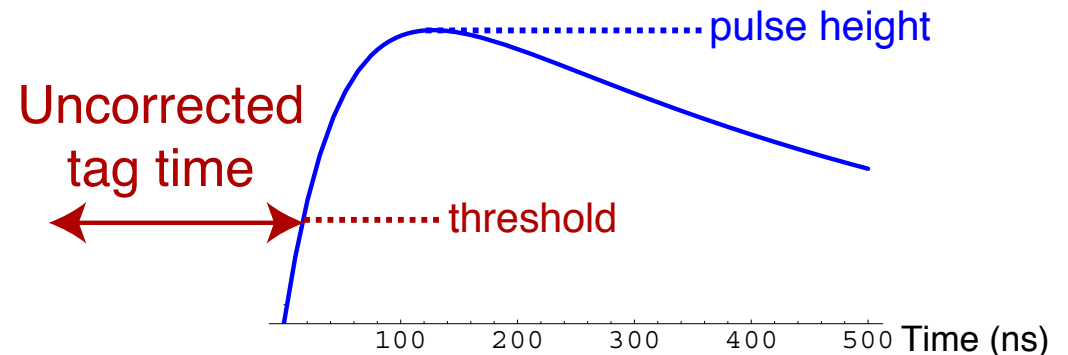
Introduction

Time tagging sufficient for low occupancy

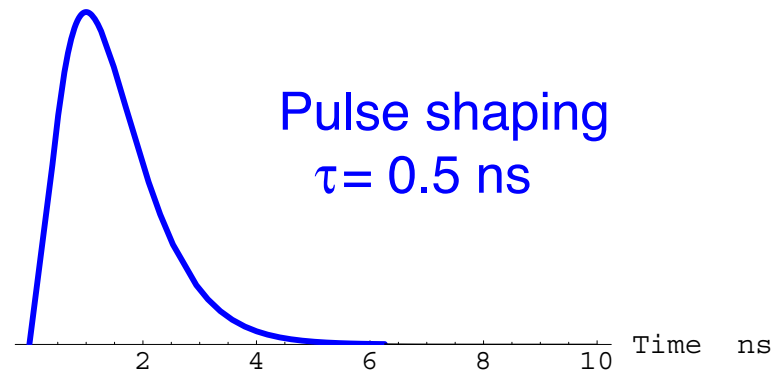
$$\sigma_t = \frac{\tau}{\text{SNR}} \left(\frac{1}{1 - \frac{a}{\text{SNR}}} \right)$$

$\tau = 50\text{ns}$, $\text{SNR}=15$, $a = 3$:

$$\Rightarrow \sigma_t = 4.7 \text{ ns}$$



Short shaping needed for high occupancy
(e.g. Pair monitor, *n.b. signals very large here.*)



So far only Si has been deployed in HEP experiments for position and energy measurements:

- Well developed technology
- Largest charge signal

GaAs was considered, but not used by LHC experiment. One challenge is impure structure (short carrier lifetime).

CVD diamonds, not yet used in an HEP experiment* but:

- Large mobility for both holes and electrons
- Uniform field (no depletion region)
- May now be commercially available in the US

* except as radiation detectors.

Properties of Semiconductor Detectors

	Si	GaAs	Diamond
Drift Mobility $\left(\frac{\mu m/ns}{V/\mu m}\right)$			
Electrons	145	850	180
Holes	45	32	120
Dielectric Constant	11.9	12.9	5.7
Mean energy for electron-hole creation (eV)	3.63	4.35	13.1
Density (g/cm ³)	2.33	5.32	3.52
Charge/ μm (electrons) (collected in experiments)	80	33 ^a	35 ^b

Notes: (i) Typical field from bias voltage is 0.5 - 1.0 V/ μm .
(ii) Dielectric constant important for detector capacitance

^a NIM A 388 (1997) 408. ^b NIM A 514 (2003) 79.

Charge Collection Times

- All materials can be biased to be fast enough for time tagging (300 μm thick material)

Material	$V_{depletion}$	V_{bias}	Ideal charge collection time	
			Holes	Electrons
Si	80V	200 V	11 ns	3.2 ns
GaAs*	80V	200 V	15 ns	0.6 ns
Diamond	-	200 V	3.8 ns	2.5 ns

* Assumes GaAs behaves as Si, reality is more complicated, see hep-ex/9509011.

- Charge collection times can be decreased by using impure material (e.g. GaAs electron lifetime of 1ns have been reported)
- For the pair monitor typical signals are $\sim 10^3$ larger and only a fraction of the charge must be collected. This can be accomplished by using thin or impure materials.

Electronics Consideration

Most sources of electronics noise have

$$\frac{1}{\text{SNR}} \propto \text{ENC} \propto C_{in} \sqrt{\frac{1}{\tau}}$$

where τ is the shaping time of the amplifier and C_{in} is the input capacitance.

Thus

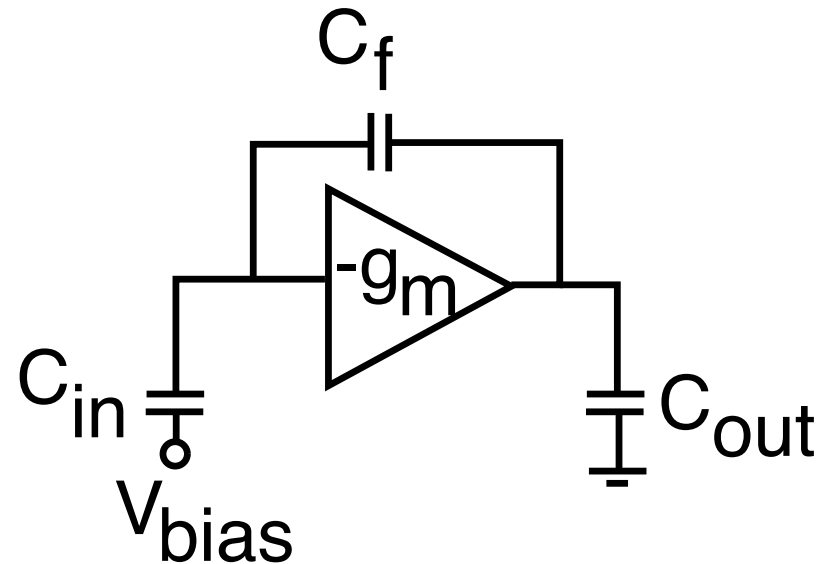
$$\sigma_t = \frac{\tau}{\text{SNR}} \left(\frac{1}{1 - \frac{a}{\text{SNR}}} \right) \propto C_{in} \sqrt{\tau}$$

provided the $\text{SNR} \gg a$

For charge amplifiers:

$$\tau \simeq \frac{C_{in}(C_{out} + C_f)}{g_m C_f}$$

where g_m is the transconductance



Thus $\sigma_t \propto C_{in}\sqrt{\tau} \propto C_{in}^{3/2}$

Obviously we want to decrease C_{in}

g_m can not be increased indefinitely to compensate for large C_{in} :

- For CMOS capacitance of input FET will eventually dominate C_{in} .
- For bipolar base current from input transistor dominate noise.

Noise contribution of an FET Amplifier

The noise from the input FET of the amplifier is

$$ENC_{FET} = \frac{C_{in}}{q_e} \sqrt{4KT \frac{2}{3g_m} \frac{1}{4\tau}}$$

Numerically

$$ENC_{FET} \simeq 320 C_{in} \sqrt{\frac{1}{g_m \tau}}$$

for C_{in} in pF, g_m in mS and τ in ns.

If the only significant source of noise is from the CMOS input transistor g_m

$$\sigma_t \propto \sqrt{\frac{C_{in}^3}{g_m^2}}$$

Since g_m is at most $\propto I_{drain}$ from an analog power point of view we are better off by making more small capacitance cells than a few large ones.

Noise contribution of bipolar logic (e.g. SiGe)

For a bipolar transistor

$$g_m = \frac{I_c q_e}{KT} \quad ENC_{collector} = \frac{C_{in}}{g_m q_e} \sqrt{2q_e I_c \frac{1}{4\tau}}$$

Numerically $g_m \simeq 40I_c \quad ENC_{collector} \simeq 44C_{in} \sqrt{\frac{1}{I_c \tau}}$

for I_c in mA, C_{in} in pF and g_m in mS.

But, shot noise due to the base can be large, especially if one integrates for an entire bunch train:

$$ENC_{base} \simeq \sqrt{\frac{I_c \tau_{int}}{\beta q_e}}$$

Numerically

$$ENC_{base} \simeq 2500 \sqrt{\frac{I_c \tau_{int}}{\beta}}$$

for τ_{int} in ns and I_c in mA.

Another important effect is the contribution of the base spreading resistance (note that strip resistances will add a similar term):

$$ENC_{R_b} = \frac{C_{in}}{q_e} \sqrt{4KT R_b \frac{1}{4\tau}}$$

For R_b in Ω s and C_{in} in pF:

$$ENC_{R_b} \approx 13 C_{in} \sqrt{\frac{R_b}{\tau}}$$

Conclusion:

- CMOS electronics will probably be used for low occupancy regions
- Bipolar SiGe looks attractive for short shaping time and high occupancy

Limitation on strip length

In tracking detectors the input capacitance will be dominated by the interstrip capacitance and the capacitance to the substrate.

For pitch p , strip width w , and silicon thickness d , the capacitances, in pF/cm, are approximately:

$$C_{intr} \sim 1.6 \frac{w+20}{p} \text{ pF/cm}$$

$$C_{sub} \sim 1.1 \frac{p}{d} \text{ pF/cm}$$

C_{intr} taken from CMS – interstrip capacitance depends on radiation and detail of implants, c.f. IEEE TNS 42 (1995)42.

Subsequent calculations include higher order terms for C_{sub}

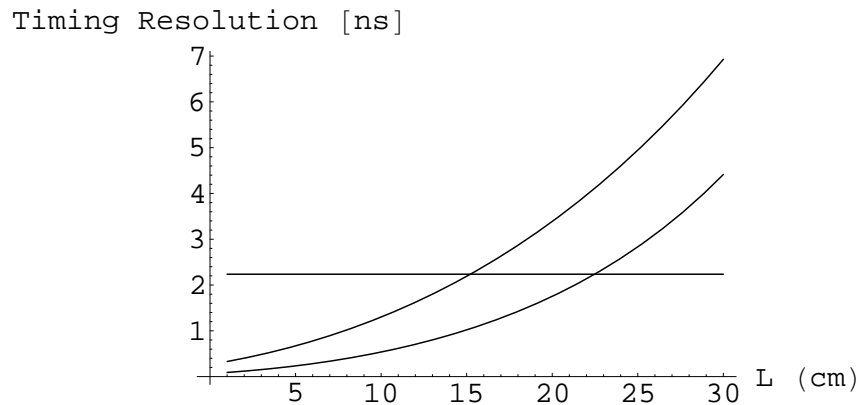
The resistance/length of the Al strips of width w and thickness h is

$$R_s = \frac{275}{w h} \Omega/\text{cm} \quad (w, h \text{ in } \mu\text{m})$$

In general strips much thicker than 1-2 μm are difficult to produce.

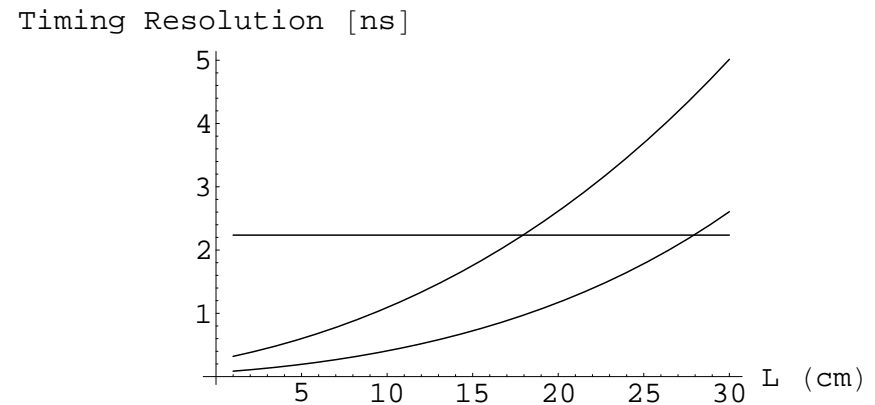
Assuming a *perfect* CMOS amplifier with $g_m = 2.5\text{mS}$ or $g_m = 10\text{mS}$ and $C_{gs} = 10\text{pF}$, we can now plot the ideal strip time resolution versus strip length, varying w to its minimum.

Minimum w typically $10\text{-}15\mu\text{m}$ for $g_m = 2.5\text{mS}$ and $1\mu\text{m}$ thick strips.



1 μm thick strips

upper curve 2.5mS, lower 10mS



2 μm thick strips

upper curve 2.5mS, lower 10mS

- Since there will be other sources of noise, these curves are lower limits on the timing resolution
- Strips 10 cm long look possible (just fits on a 6in wafer)
- Strips 20 cm long might be possible for $2\mu\text{m}$ thick Al strips

A note on power: warm versus cold

- An example: ECAL CMOS Front end electronics, 1024 channels, total time to ramp up and down: $9\mu\text{s}$.

- Instantaneous power is high, but average is low:

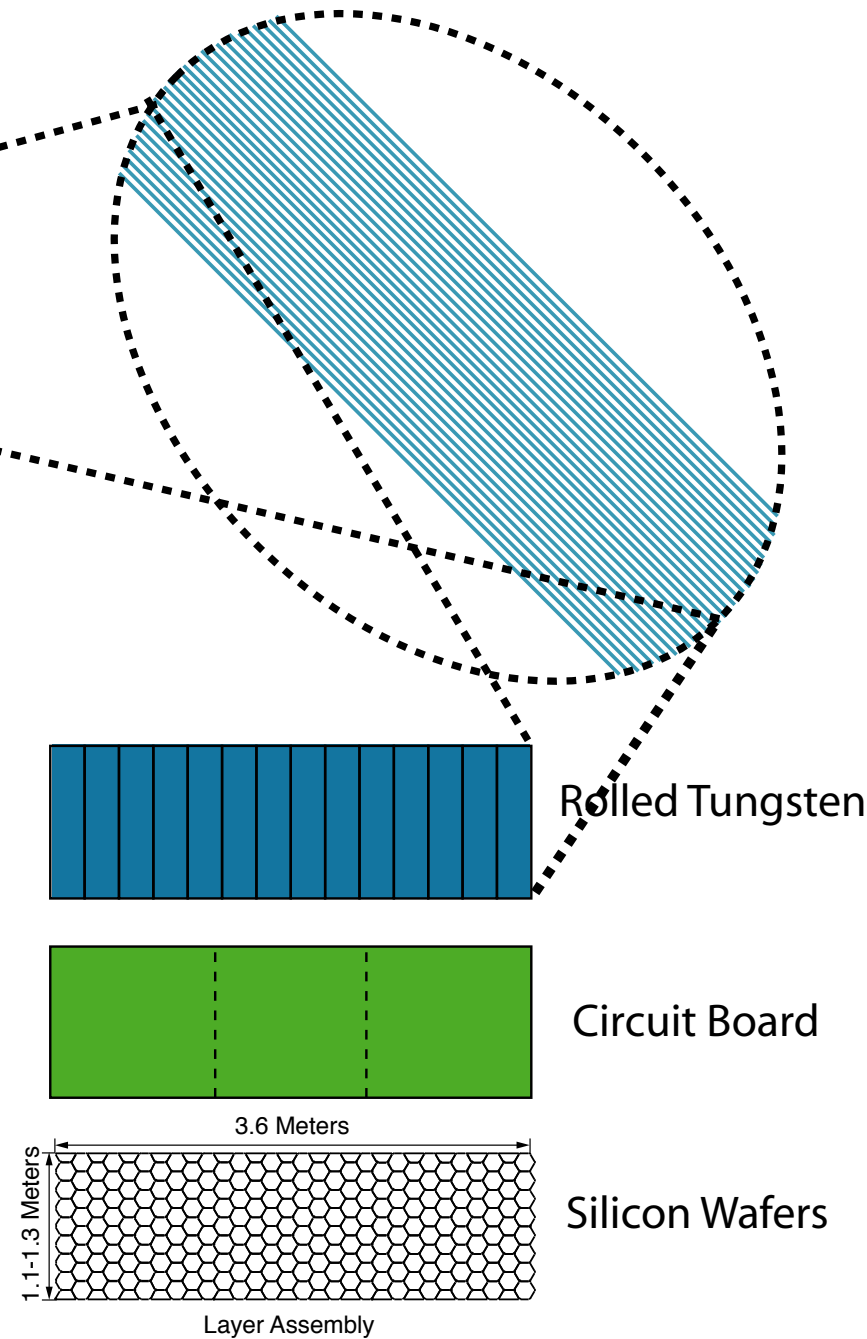
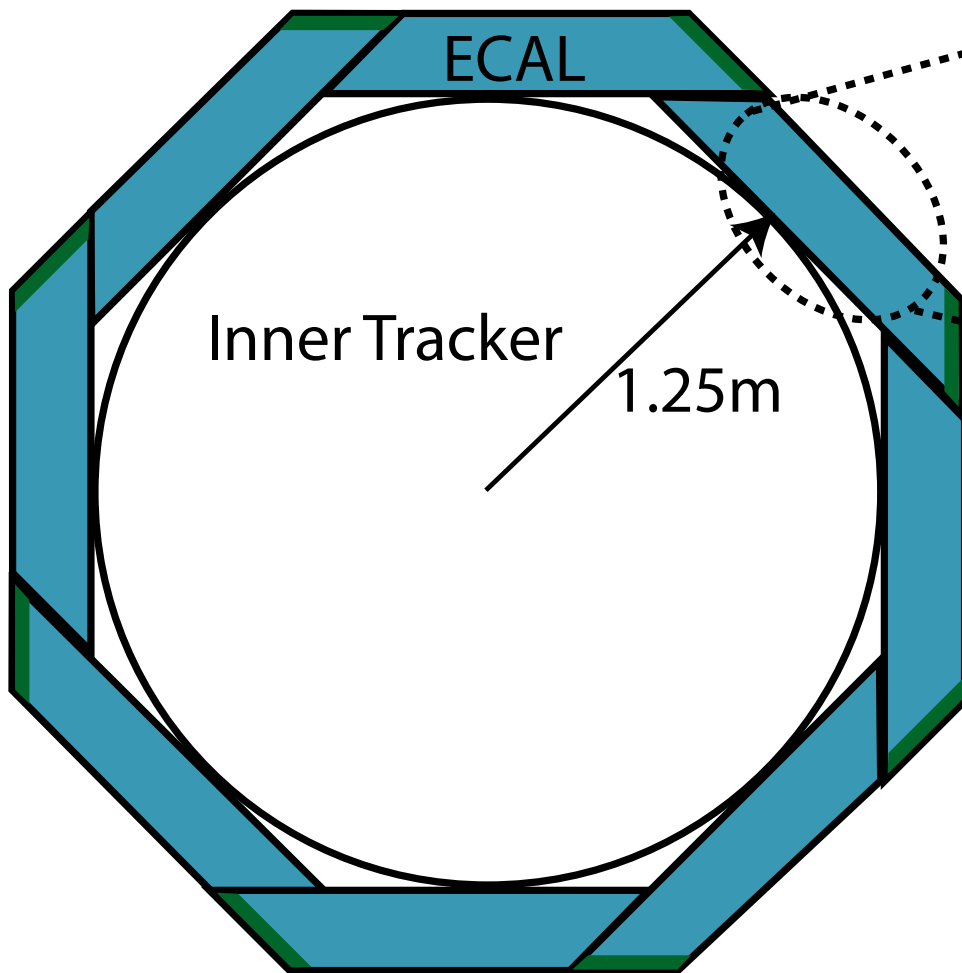
	Instantaneous	Average Warm	Average Cold
Analog charge amp	1000 mW	1.1 mW	5.0mW

⇒ Power pulsing allows for low average power.

- Average digital power and standby analog power dominates ($\sim 30\text{mW}$)
- Instantaneous analog power in warm machine can be increased with small impact

Average digital power depends on total number of ADC conversions, this is likely to be similar for warm and cold. If ever bunch crossing is digitized, it will be much larger for cold.

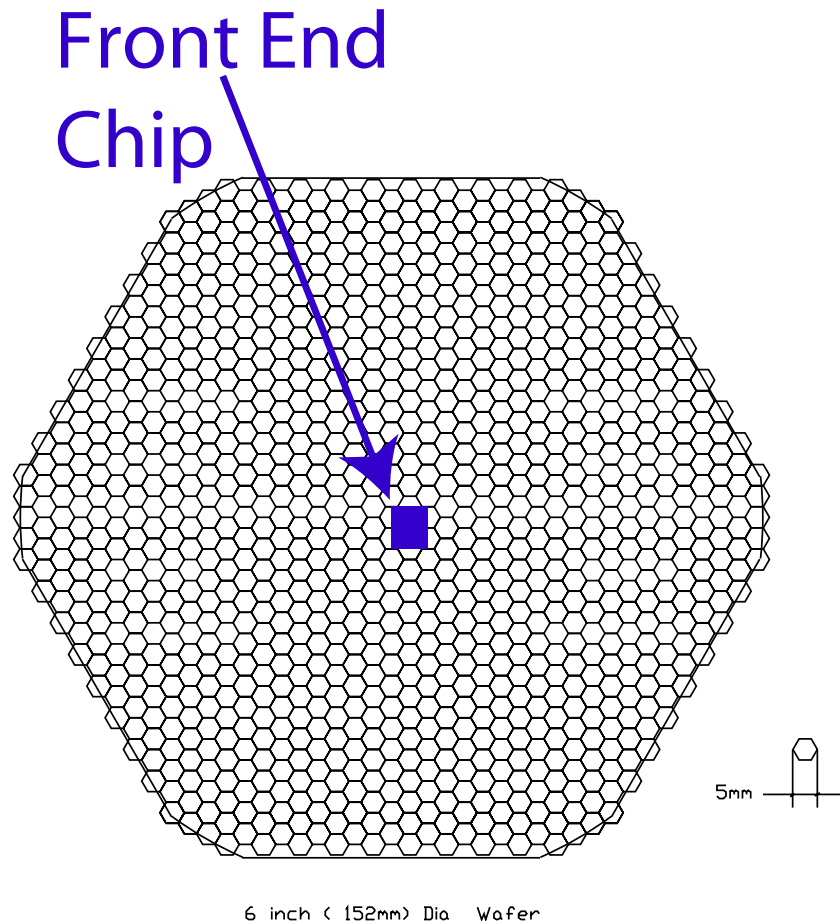
Si-W Calorimeter Concept



Transverse Segmentation $\sim 5\text{mm}$
30 Longitudinal Samples
Energy Resolution $\sim 15\%/E^{1/2}$

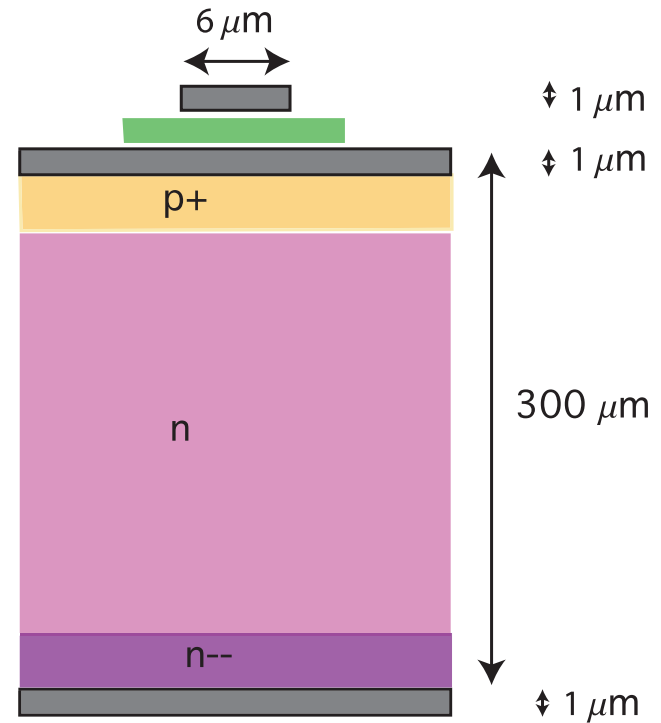
Silicon Concept

- Readout each wafer with a single chip
- Bump bond chip to wafer
- To first order cost independent of pixels /wafer
- Hexagonal shape makes optimal use of Si wafer
- Channel count limited by power consumption and area of front end chip
- May want different pad layout in forward region



Silicon Design Details

- DC coupled detectors (avoids bias resistor network)
- Two metal layers
- Keep Si design as simple as possible to reduce cost
- Cross talk looks small with current electronics design
- Trace capacitances (design: max 15pF) are bigger than the 5pF pixel capacitance

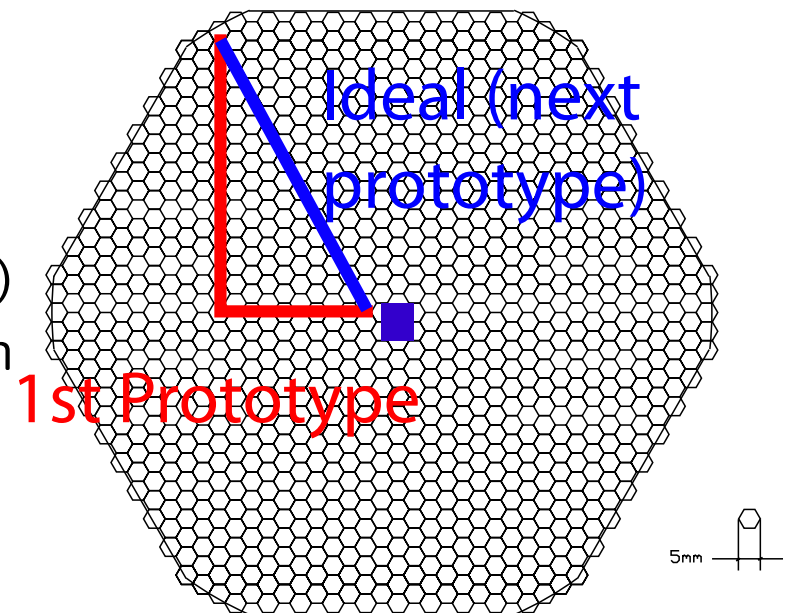


Factors limiting capacitance

- Oxide thickness, trace width:

Oxide	Oxide thickness	Trace width	Group	Si Manufacturer
SiO ₂	3-5 μm	6-8 μm	CLEO III	Hamamatsu
SiO ₂	4-5 μm	6 μm	DELPHI	Hamamatsu
SiO ₂	4 μm	xxx	H1	CSEM
SiO ₂	5 μm	8 μm	Belle	Hamamatsu
ONO	1.2 μm	12 μm	Phobos	ERSO(Taiwan)

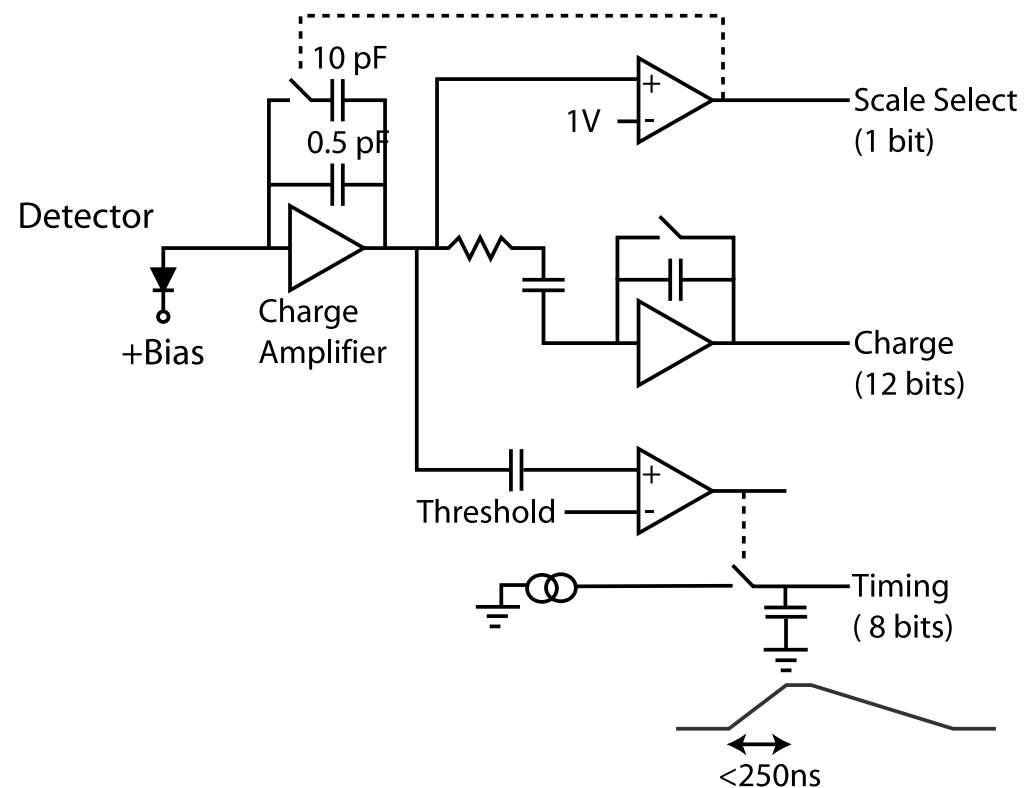
- Trace length (not ideal in first prototype) subsequent calculations assume max length 7cm ($R = 350 \Omega$)



Electronics Design

- Novel design due to D. Freytag uses two different feedback capacitors
(NB: same scheme independently developed by the Pamela cosmic ray group in Italy)
- 5 to 10ns timing possible
- Current in input transistor pulsed, *duty cycle* $< 10^{-3}$
- Expect power $\ll 40\text{mW/wafer}$
- For large signals:

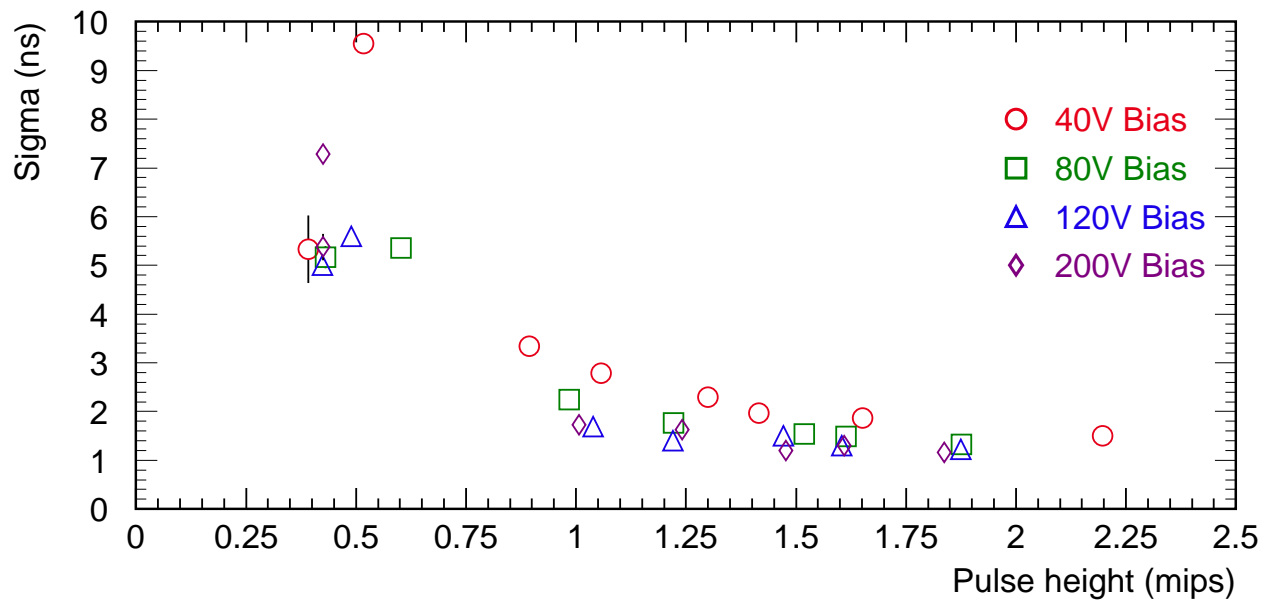
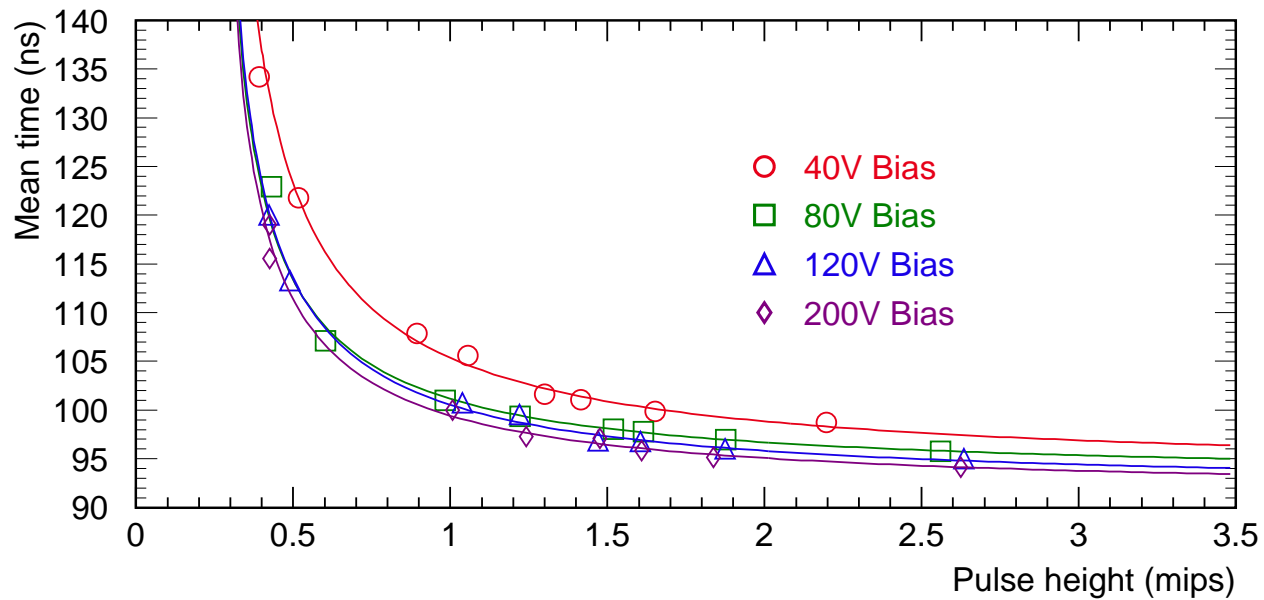
$$C_{eff} \sim \text{Gain} \times 10\text{pF}$$



Some lab measurements

- Uses Hamamatsu detectors with almost same design as LC detectors. Total capacitance much larger (40 to 50)pF due to cables and larger pad size.
- Readout electronics has similar properties to LC electronics, but somewhat larger g_m (precise value not known).
- Noise term from series resistance not precisely known
- Overall signal to noise is ~ 15

Infrared laser results (pulse shape very similar to cosmic rays):

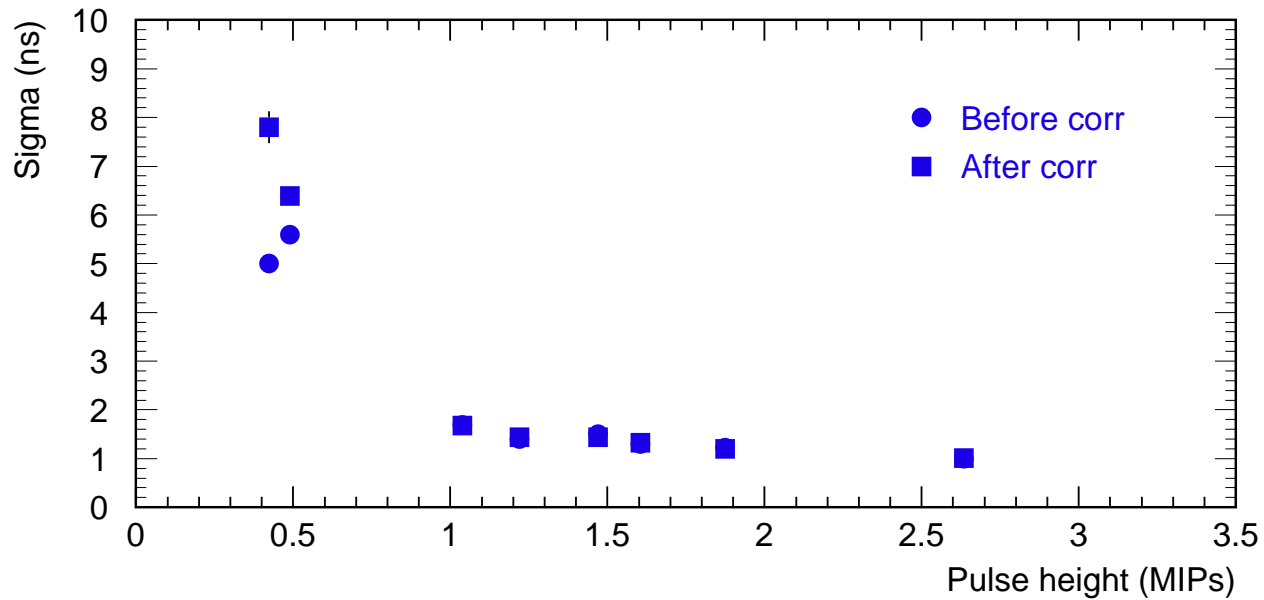
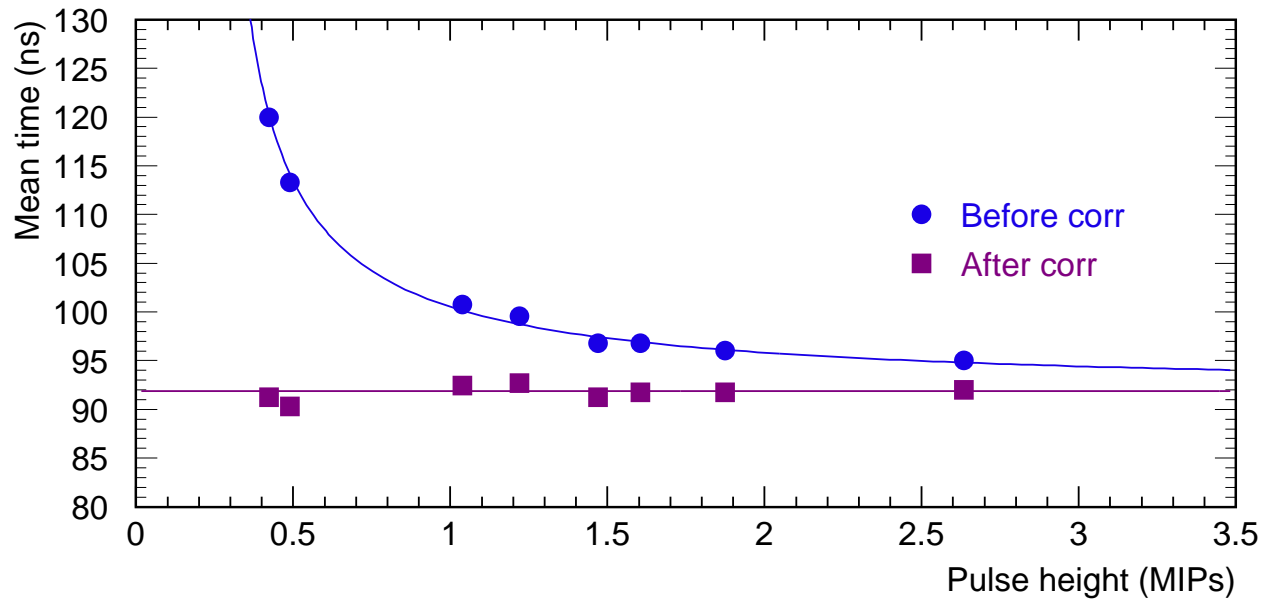


Pulse Rise Times and Collection Times

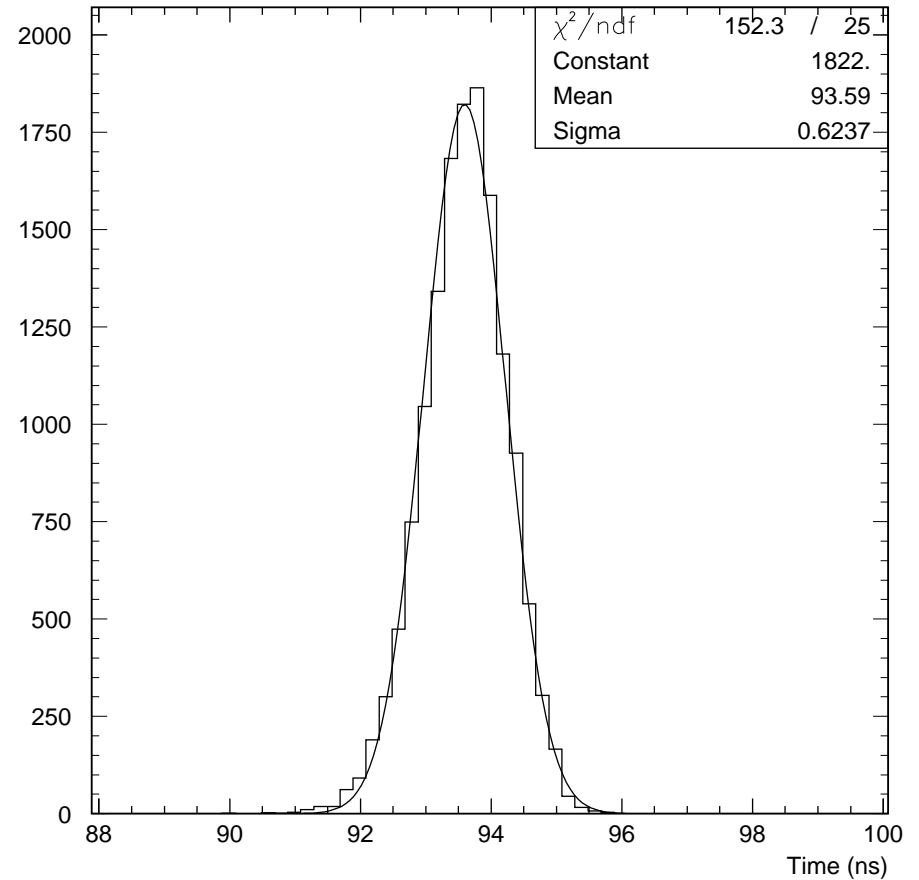
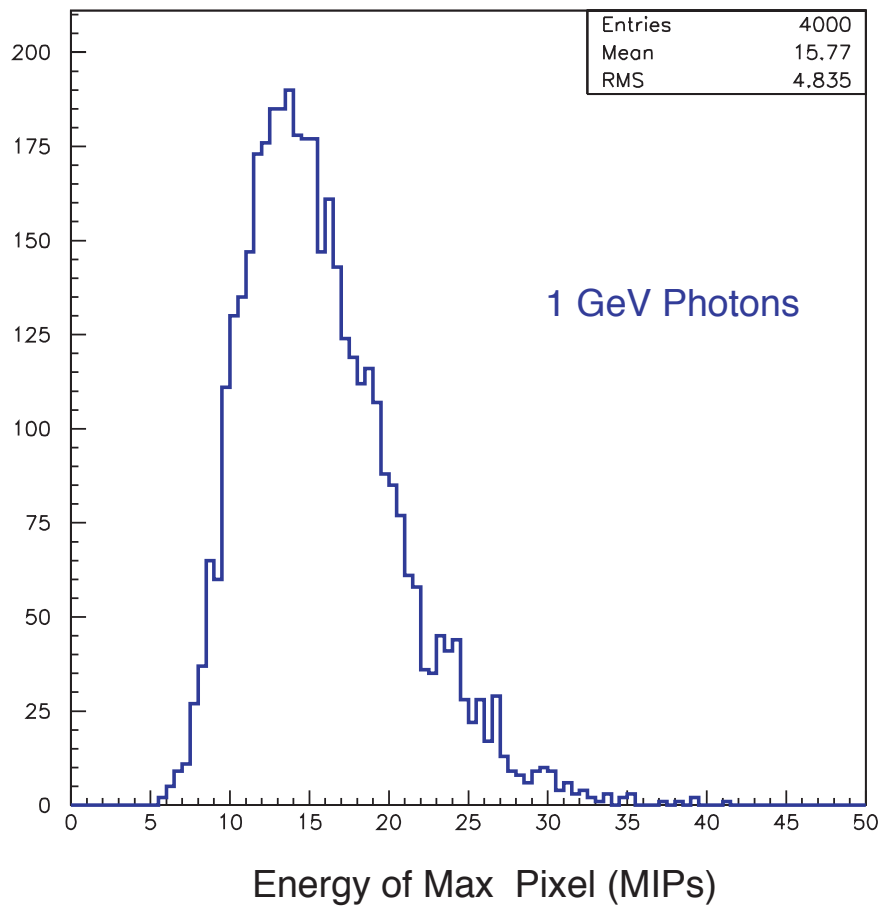
Bias voltage	τ	Theoretical collection time	
		electrons	holes
40 V	37.5 ± 0.2 ns	-	-
80 V	25.6 ± 0.1 ns	8.2 ns	25.6 ns
120 V	27.3 ± 0.1 ns	5.2 ns	15.9 ns
200 V	25.1 ± 0.1 ns	3.0 ns	9.3 ns

(Errors statistical only)

Time walk correction possible



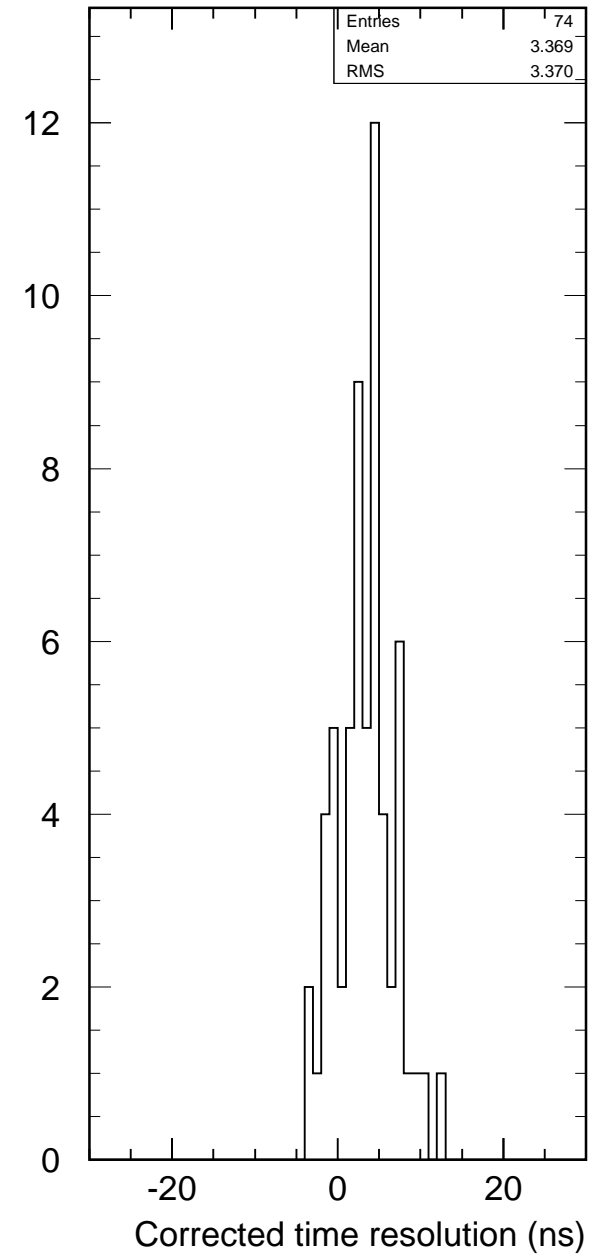
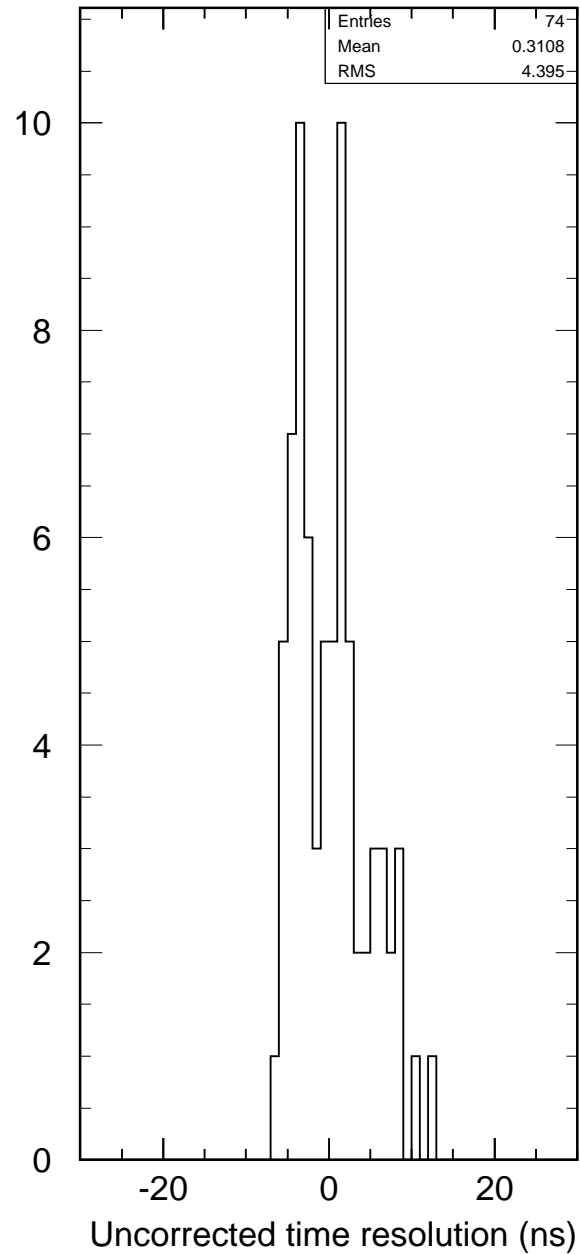
- Very large signals also have good resolution
- 6 MIP energy depositions are common in \sim GeV showers



Results for cosmic ray coincidence of 1 cm² pads with 0.25cm x 2cm detector →

Resolution is 3.4 ± 0.4 ns, better than 5ns goal.

The plot shows coincidences with both pulse heights at least 0.58 MIPs.

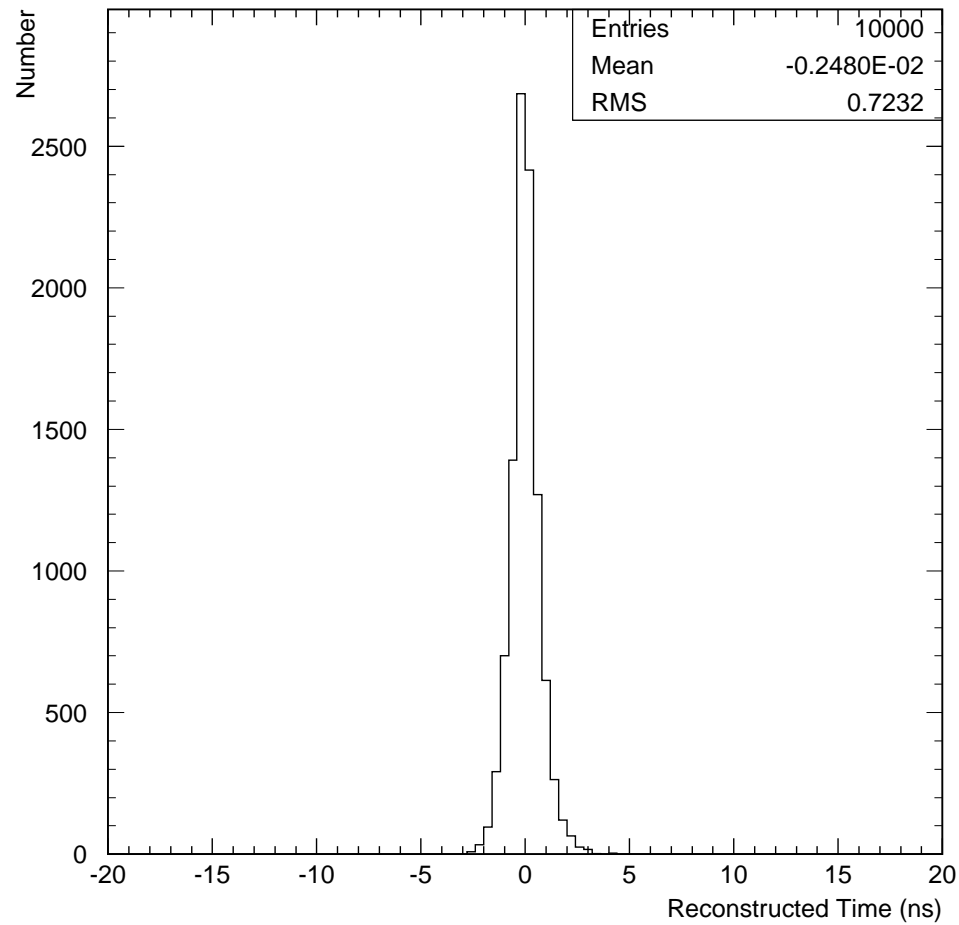


Toy Monte Carlo Studies of Timing Resolution for 30 Samples

Assumptions:

- Each MIP has 30 samples at random distances from the read-out chip
- Threshold for timing measurement is 8,000 electrons.
- Input FET has $g_m = 1.5\text{mS}$ and the noise contribution from the rest of the amplifier is equal to input FET.
- Maximum trace length 7cm (350Ω , 15pF)
- Time constant for charge measurement is 200 ns.
- Time constant for the time measurement is 50 ns **(Fixed)**.
- The noise signals in the timing and charge circuits are uncorrelated
- Random 5% channel to channel variation in threshold
- Random 1% event-to-event variation in threshold
- Random 5% uncertainty in constants used for correction.
- Reject time measurements far from mean

Results of truncated mean for 30 samples



Conclusions:

⇒ **A Si tracker with 5 layers and 10 cm strips can produce a time measurement of ~ 1 ns resolution for tracks.**

⇒ **Present design of calorimeter electronics seems up to the job and can produce a measurement of with better than 1 ns resolution for MIPs.**

● **Need to demonstrate with ASIC prototype**

⇒ **Design of the silicon detectors requires some additional optimization for timing.**

⇒ **Impact of cross talk on time resolution needs more study.**