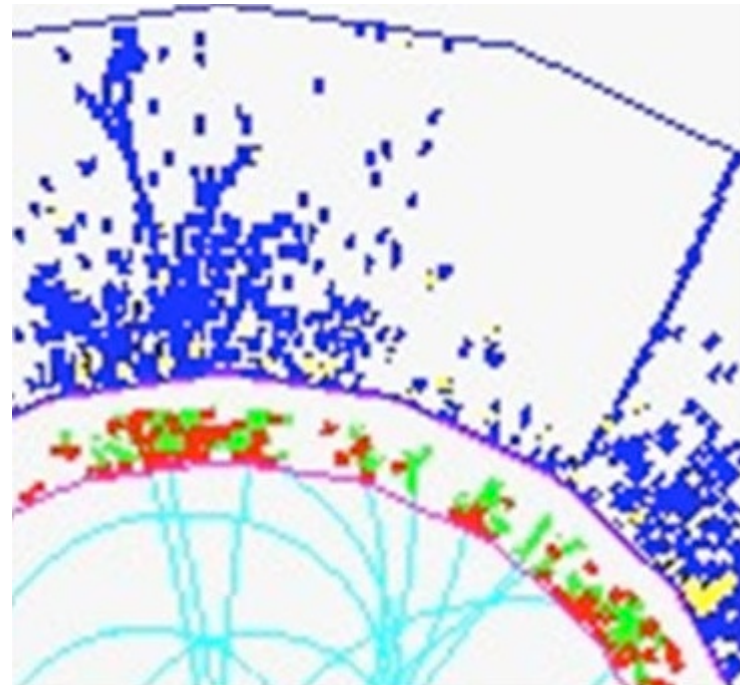


Silicon/Tungsten ECal for the SD Detector – Status and Progress

R. Frey
U. Oregon

UT Arlington, Jan 10, 2003



Outline

- Physics Goals for ECal
 - Resolution requirements
- R&D for the Si/W ECal for SD
 - Description
 - EGS4 model
 - Required simulation studies
 - Plans

ECal Goals

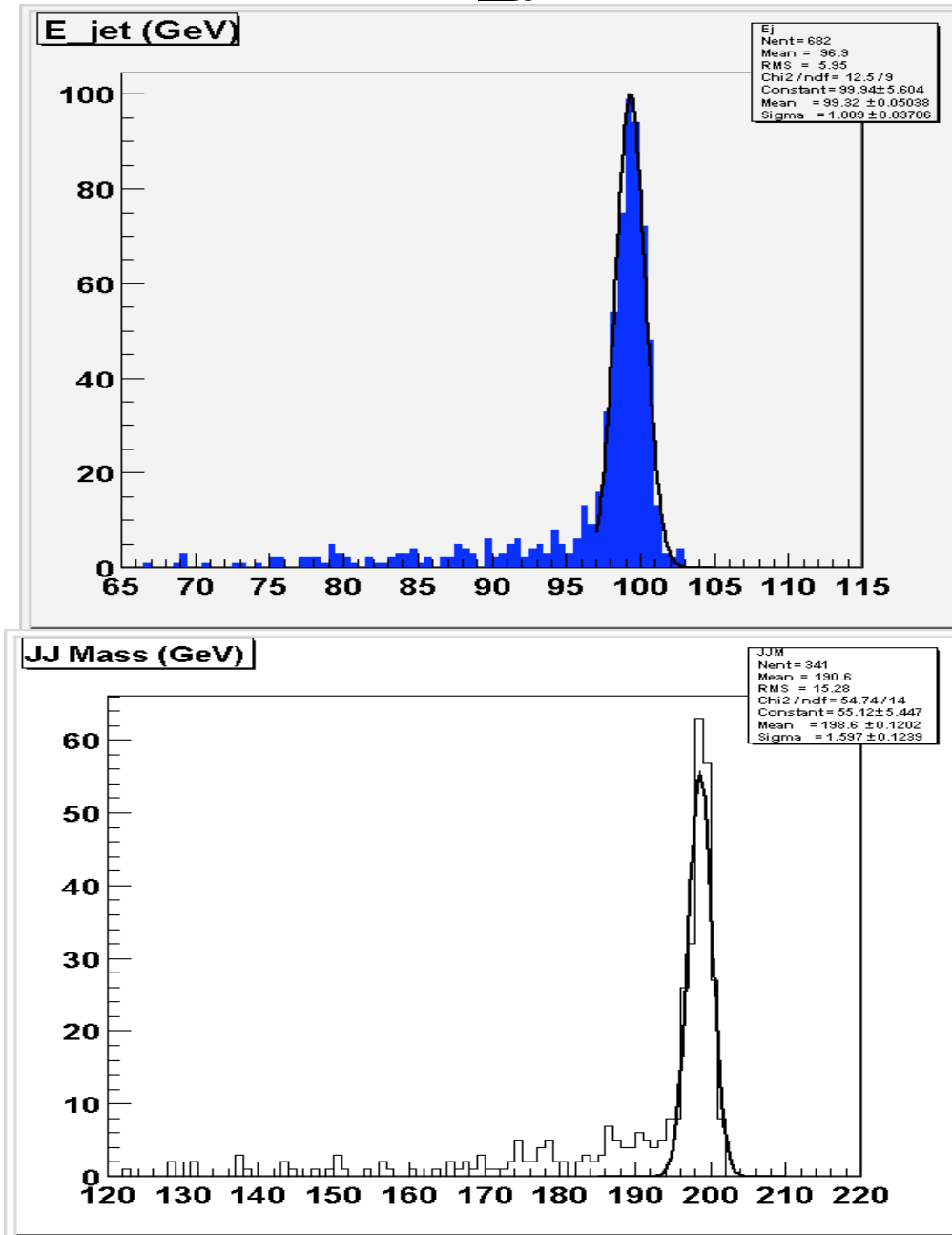
- Photons in Jets
 - Id. with high efficiency and measure with reasonable E resolution
 - ... in a very busy environment. Demand eff>95% with high purity
- Photon shower imaging
 - □ vertexing (impact param. resolution □1 cm)
 - □°_□□
 - Separation from nearby photons, MIPs, h-shower fragments
- MIP tracking (h^\pm , muons)
 - Id. Hadrons which shower in ECal
- Reconstruction of taus (eg $\tau \rightarrow \mu + \nu_\tau + \nu_\mu + \text{mip}$)
- b/c reconstruction – include neutrals in M_Q estimate
- e's and Bhabhas – easy (readout dynamic range)
 - Need to revisit requirement for Lum. spectrum
- Backgrounds immunity
 - Segmentation
 - Timing

SD Si/W Features

- Moliere radius: 9mm x (σ^2)
- Transverse segmentation almost independent of cost within reasonable range (watch thermal load)
 - Segmentation < Moliere radius _ no problem
 - Readout channels \approx detector pixels/1000
- Radiation damage probably non-issue (neutrons?)
- Timing “easily” possible with resolution of 10-20 ns
- Dynamic range OK
- Thermal management: Take advantage of low LC duty cycle
- Flexible long. sampling: Energy resolution vs Money

What are limiting contributions of calor. to jet resolution?

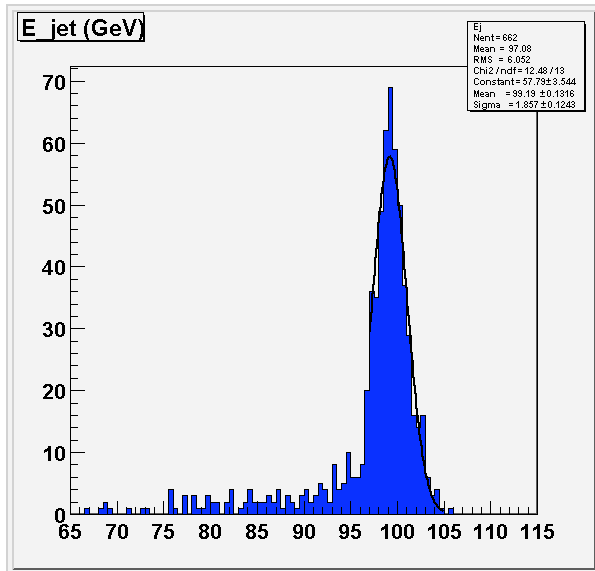
$e^+e^-_{jj}$, 200 GeV; LCDRoot FastMC



- Perfect pattern recog.
- $0.01/\sqrt{E} \oplus 0.01$ (EM)
- $0.01/\sqrt{E} \oplus 0.01$ (HAD)

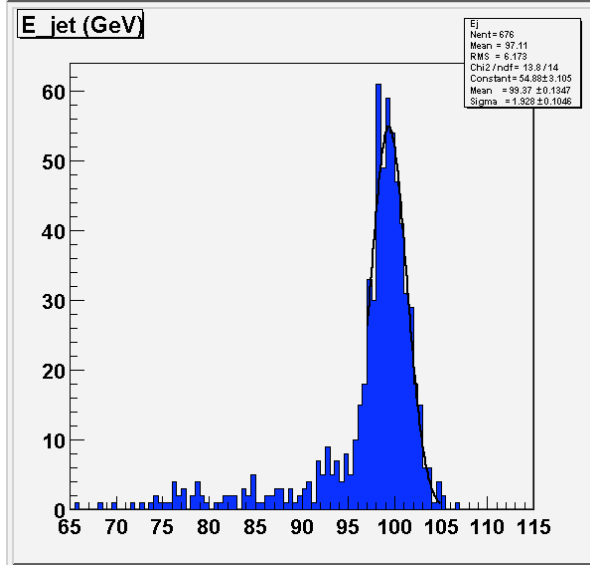
— $0.10/\sqrt{E_j}$

— $0.11/\sqrt{M_{jj}}$

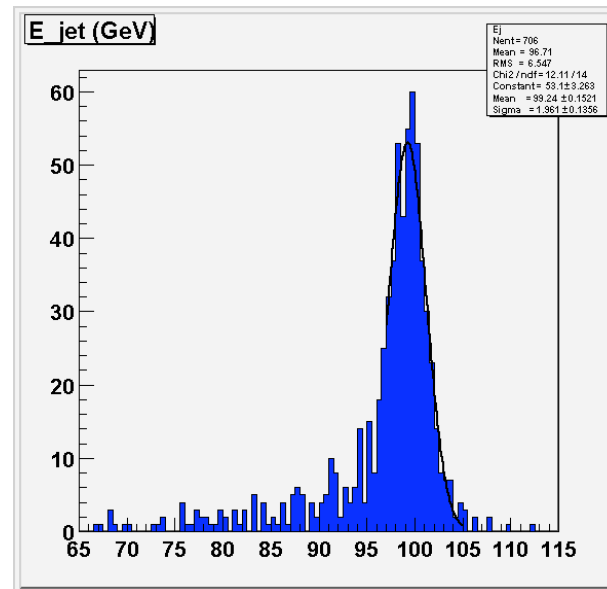


EM: $0.12/\sqrt{E} \oplus 0.01$
 HAD: $0.50/\sqrt{E} \oplus 0.02$

□ $0.18/\sqrt{E_j}$

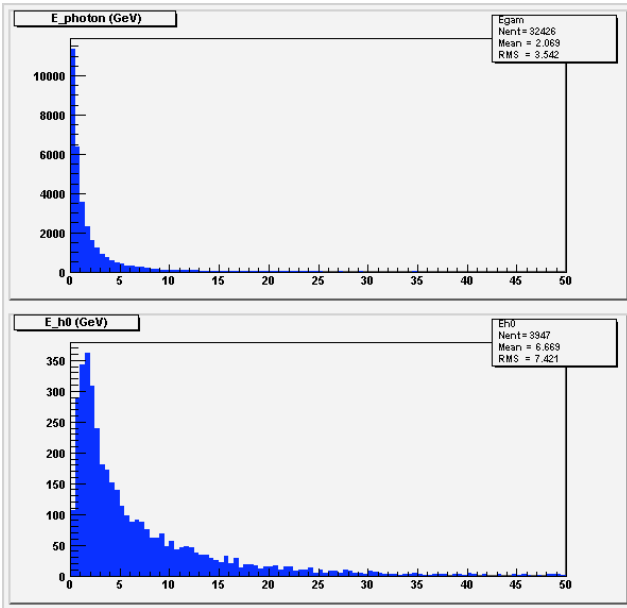


EM: $0.20/\sqrt{E} \oplus 0.01$
 □ $0.19/\sqrt{E_j}$



HAD: $0.70/\sqrt{E} \oplus 0.02$

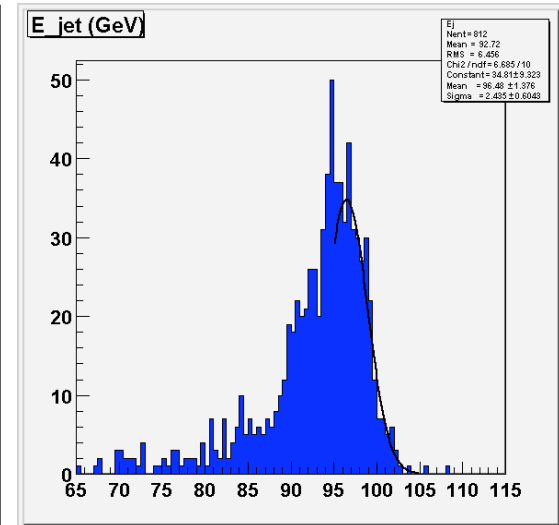
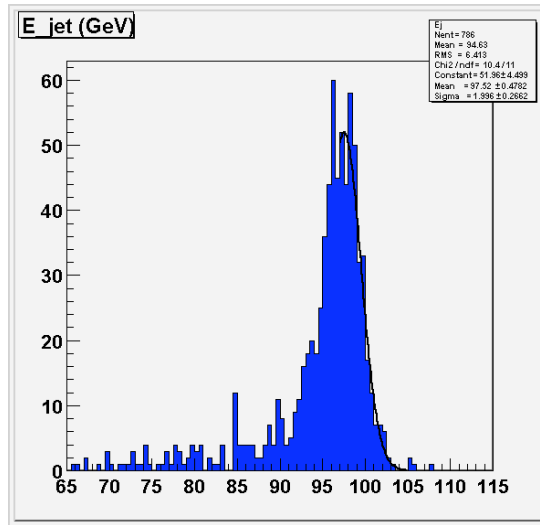
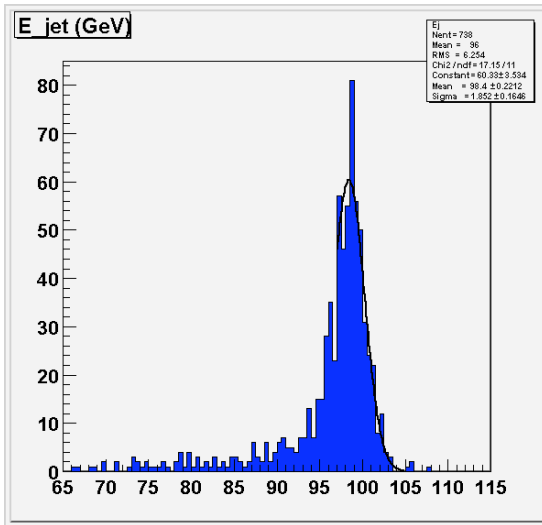
□ worse



E_{γ}

E_{h0}

What is minimum energy required for reconstructing neutrals in jets?



$E_{\gamma} > 0.5 \text{ GeV}$
 $\sigma \approx 0.19/\sqrt{E_j}$

$E_{\gamma} > 1 \text{ GeV}, E_{h0} > 1 \text{ GeV}$
 σ worse

$E_{\gamma} > 2 \text{ GeV}$
 σ terrible

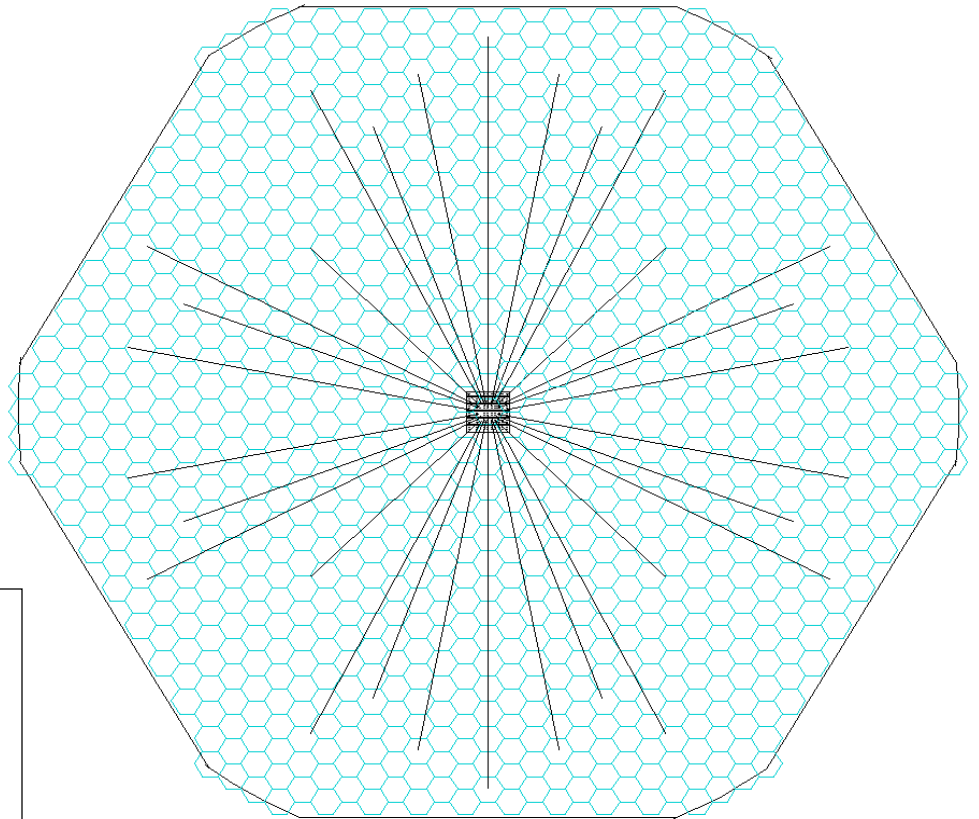
SD Si/W

- 5x5 mm² pixel □ 50M pixels
 - For each (6 inch) wafer:
 - 1000 pixels (approx)
 - One readout chip – analog and dig
 - Simple, scalable detector design:
 - Minimum of fab. steps
 - Use largest available wafers
- Detector cost below \$2/cm²
- Electronics cost even less
- **A reasonable (cheap?) cost**

M. Breidenbach, D. Freytag, G. Haller, M.
Huffer, J.J Russell
Stanford Linear Accelerator Center

R. Frey, D. Strom
U. Oregon

V. Radeka
Brookhaven National Lab

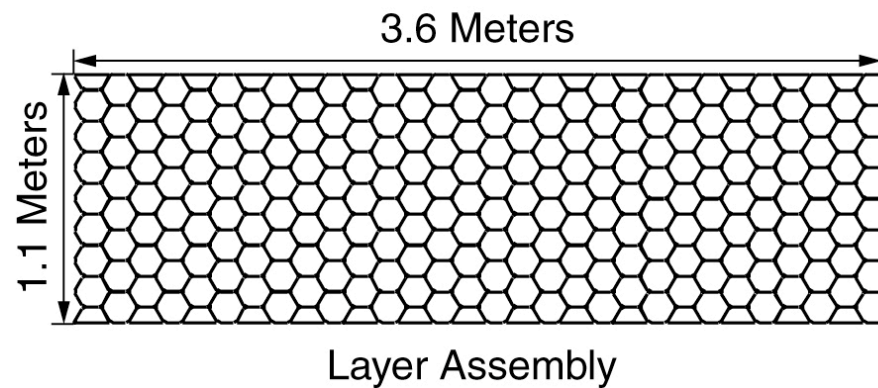
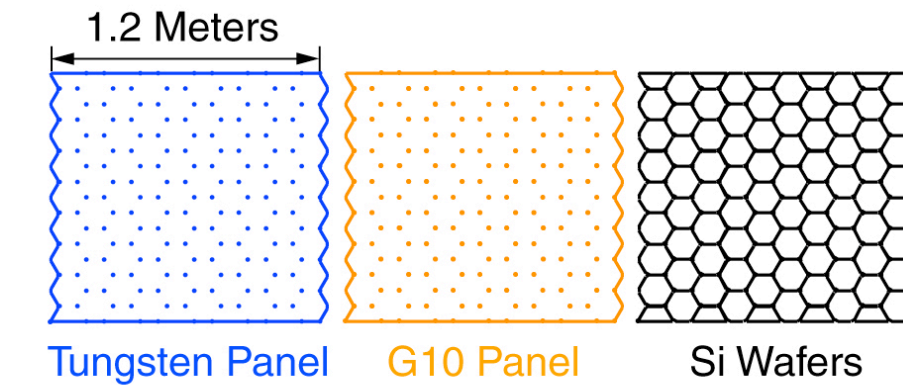


6 inch (152mm) WAFER

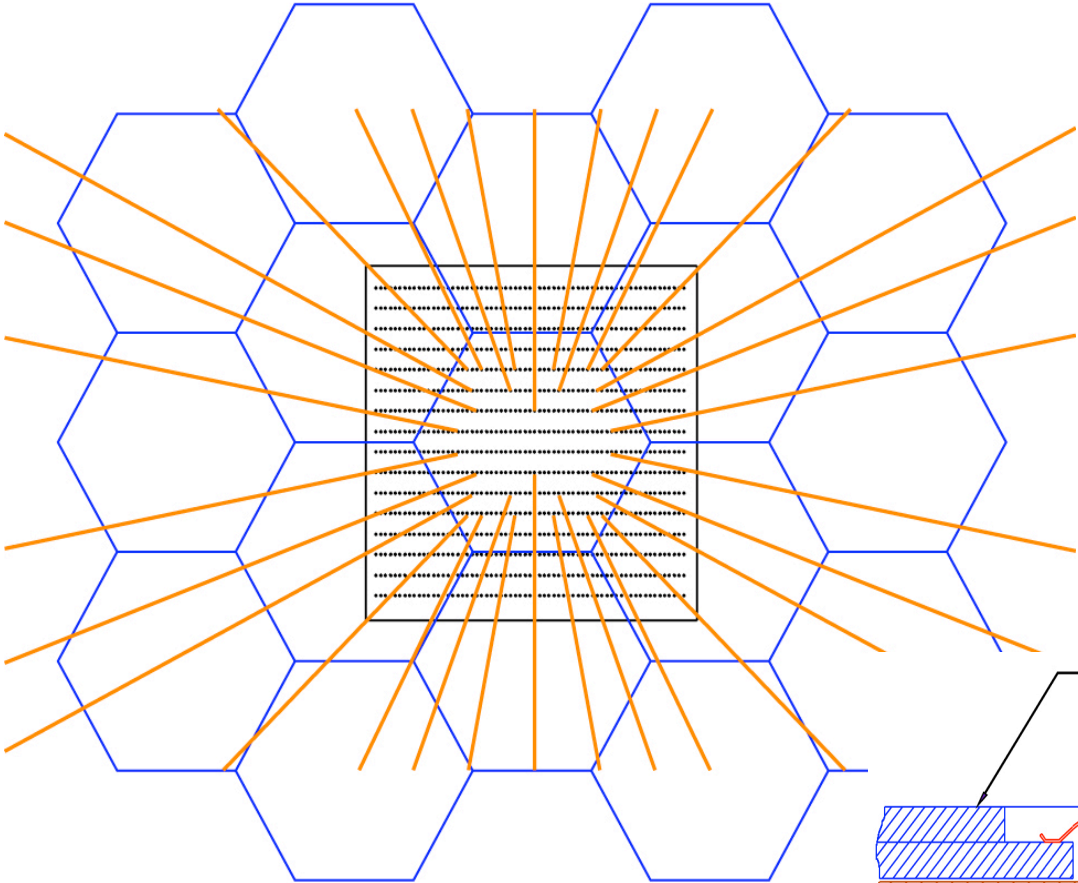
1,027 (5mm) CELLS

Putting together a layer

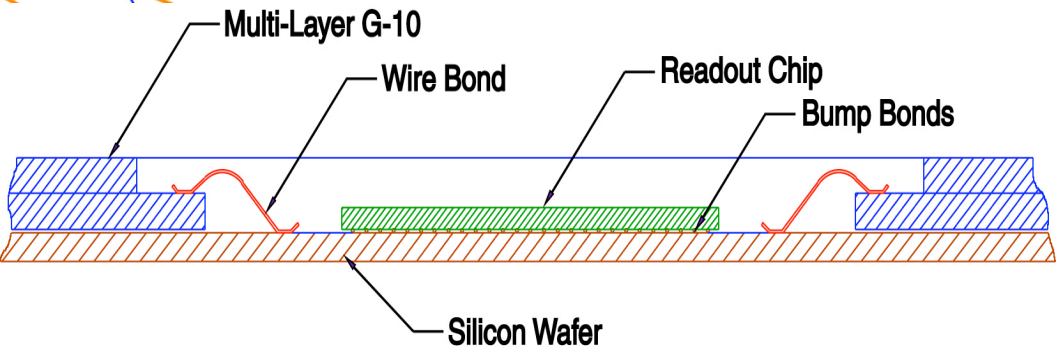
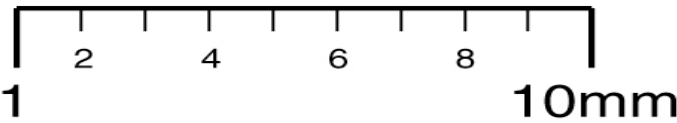
Calorimeter Layer



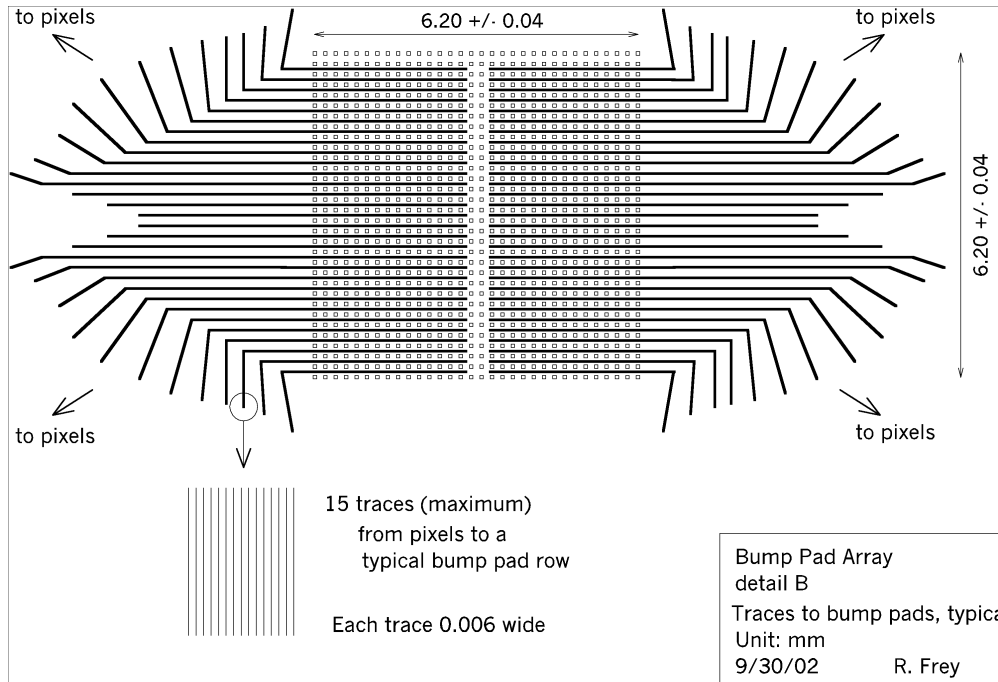
Wafer and readout chip



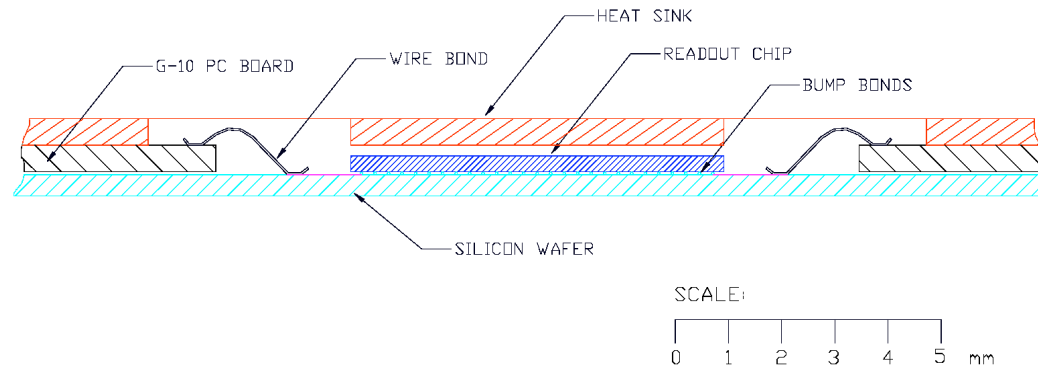
Use bump-bonding technique to mate ROC to array of pads on wafer



Readout chip connections

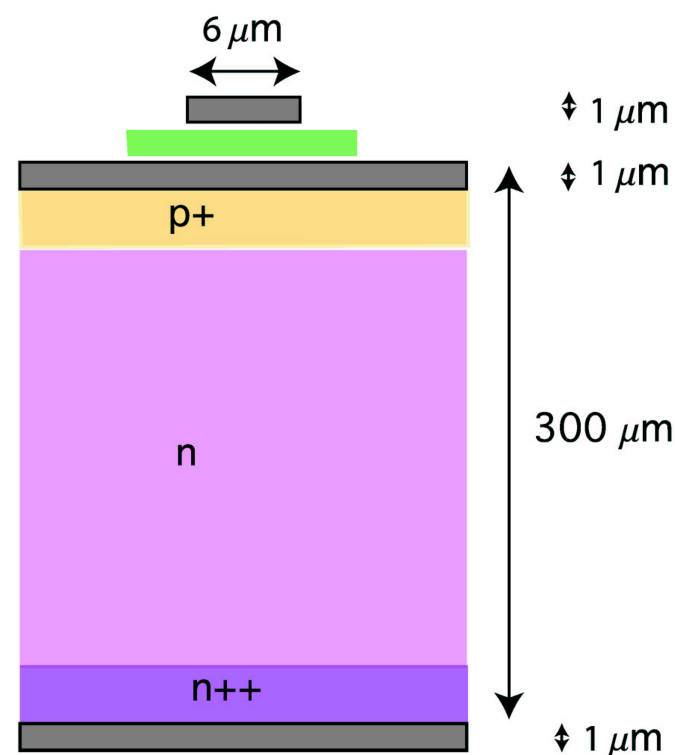


Use bump-bonding
technique to mate ROC to
array of pads on wafer



Silicon detector layout considerations

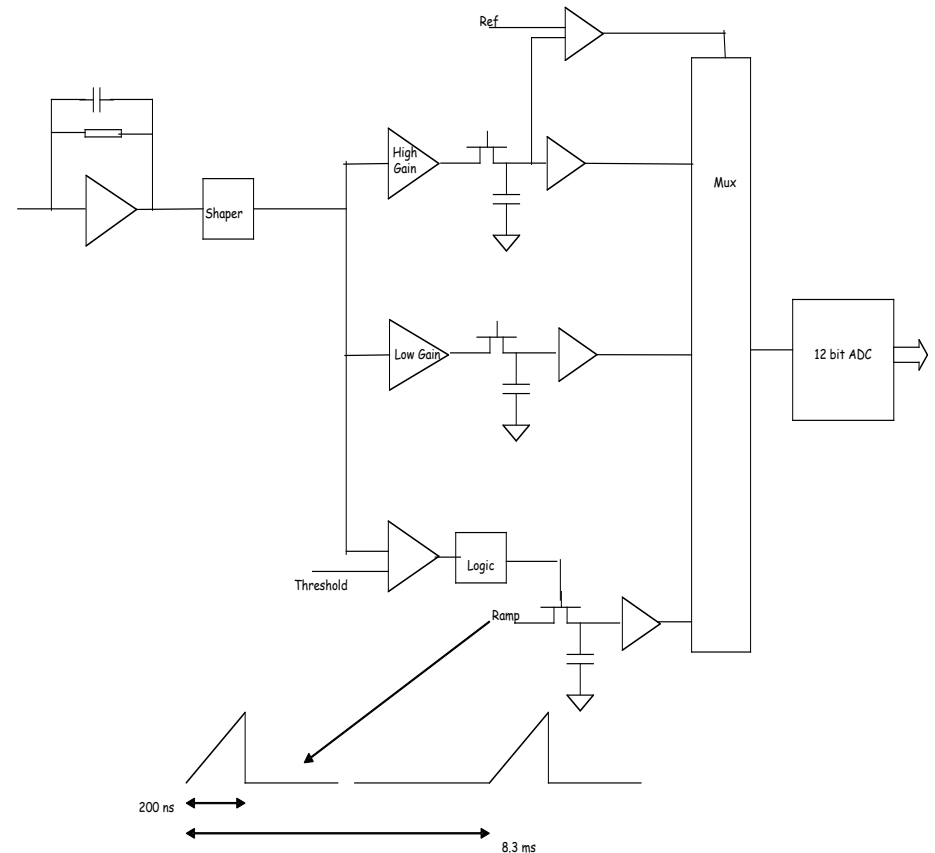
- DC coupled detectors are simple (cheap)
 - Used at LEP with AMPLEX-type preamp design
 - OK as long as leakage currents small and *stay* small
 - Straightforward layout uses two metallization layers (OK)
 - Maximum pixel-readout trace crosstalk is 0.5% (6 μm strip width and 3 μm oxide)
- AC coupled also possible
 - Avoid inputting leakage current to preamp
 - More complicated
 - Complete additional network (hard)
 - Additional layer and vias
 - Cap. breakdown
 - Beware hierarchy of capacitances



□ DC

Electronics...New: Timing

- Dynamic range: MIPs to Bhabhas
 - 500 GeV Bhabha/MIP \approx 2000 (1 pixel)
 - Want to maintain resolution at both ends of scale
- Timing: What do we need?
 - NLC: 270 ns bunch trains – Do we need to resolve cal. hits within a train?
 - Bhabhas: 15 Hz for >60 mrad at 10^{34}
 - What about 2-photon/non-HEP background overlays?
 - Exotic new physics signatures



□ Can try to provide timing for each pixel

Is ≈ 10 ns resolution sufficient ?

Radiation

- EM radiation dominated by Bhabhas (in forward endcap)
 - $d_{\text{t-channel}}/d\theta \approx 10 \text{ pb}/\theta^3$ for t-channel
 - Consider 1 ab^{-1} , 500 GeV, shower max., and $\theta=60 \text{ mrad}$ (worst case)
 - Use measured damage constant (Lauber, et al., NIM A 396)
 - $\approx 6 \text{ nA}$ increase in leakage current per pixel
 - Comparable to initial leakage current
 - Completely negligible except at forward edge of endcap
- Evaluation of potential neutron damage in progress
- A 300 GeV electron shower into a readout chip?
 - “Linear Energy Threshold” (LET) is 70 MeV/mg/cm^2
 - 1 MIP in Si: 1.7 MeV/g/cm^2
 - Expect no problems (check)

Heat

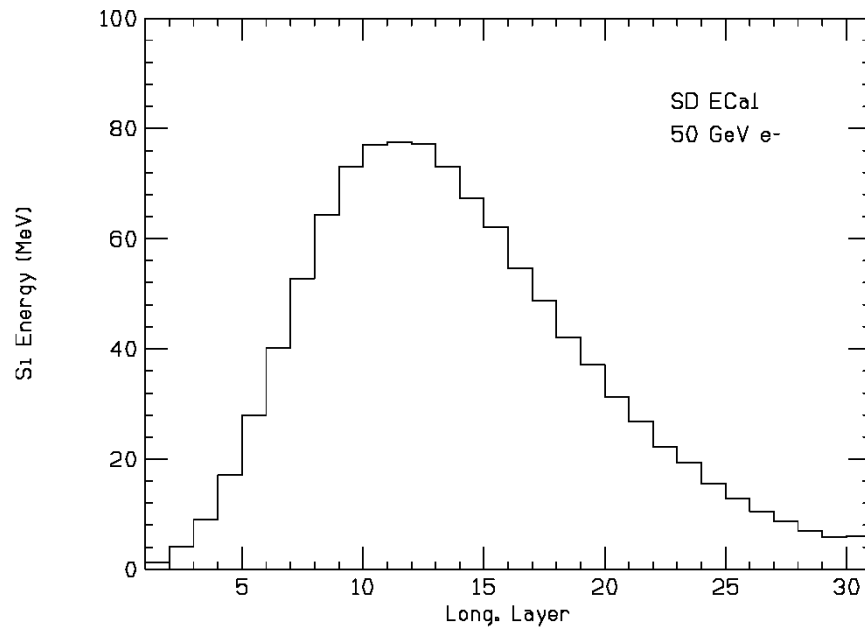
- Does integrated design imply fancy cooling system?
- Consider: NLC duty cycle is 5×10^{-5} (5×10^{-3} for TESLA)
 - 270 ns bunch trains at 150 Hz
- Use power pulsing of the electronics
- For example, GLAST-equivalent readout would produce only about 1 mW average power per 1000-channel chip
 - Assumes power duty cycle of 10^{-3}
... this factor is an important R&D item
- Current proposed scheme:
 - Heat conduction thru thick (6 oz) Cu layer in G10 m-board to fixed temperature heat sinks at edges of ECal modules
- Requires R&D to demonstrate

EGS4 Model

- Why? Check Geant4. (Thin sampling layers (Si) tricky.)
- Longitudinal
 - Energy resolution
 - Sampling/cost optimization
- Transverse
 - Effective Moliere radius
 - Dynamic range
- Hit occupancy for Bhabhas

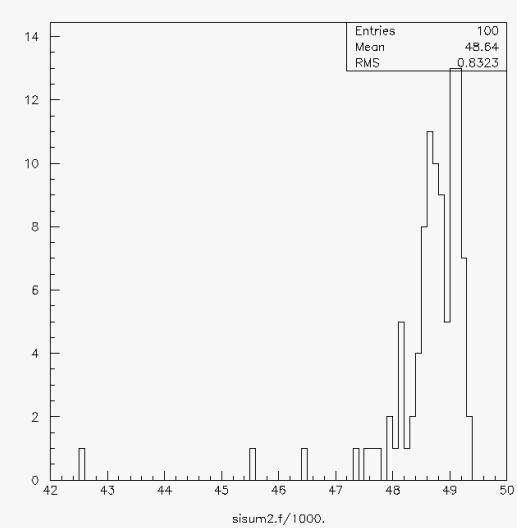
Standard SD: 30 Layers, 20 X_0 .

50 GeV electrons

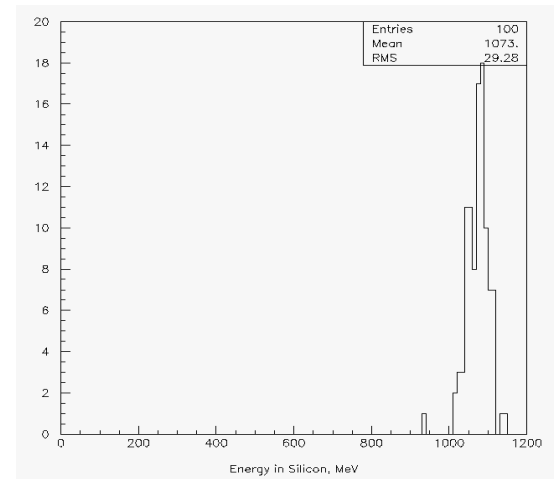


$$\sigma_E / E \approx 0.16 / \sqrt{E}$$

Total Absorbed Energy

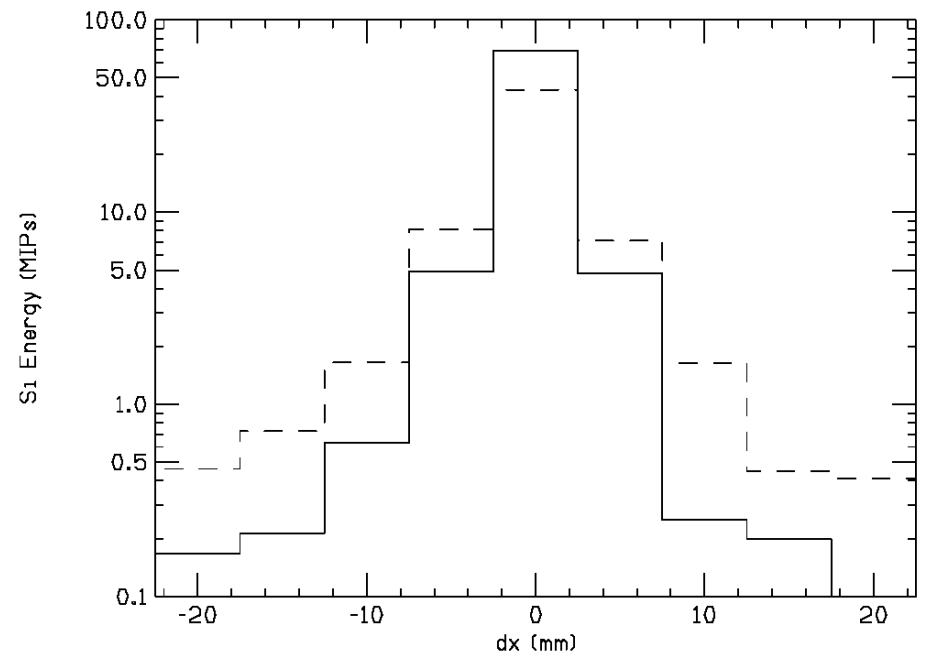
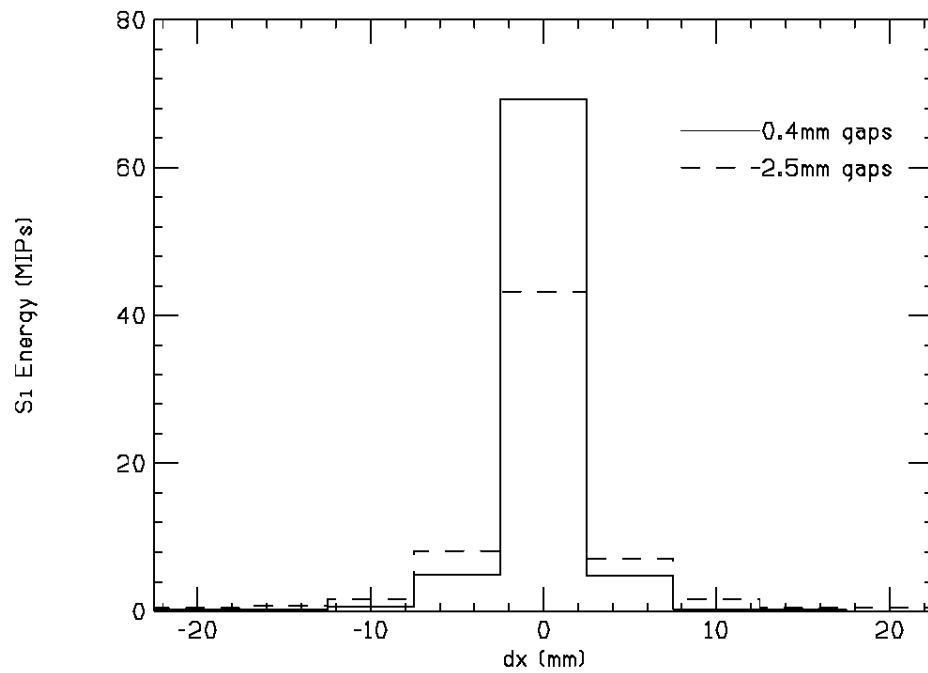


Total Energy in Si



Effective Moliere radius

- Standard SD: 5x5 mm² pixels with (1) 0.4mm or (2) 2.5mm readout gaps.
- 10 GeV photons; look at layer 10

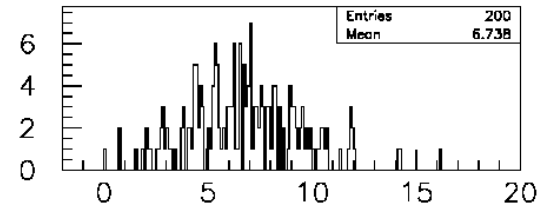
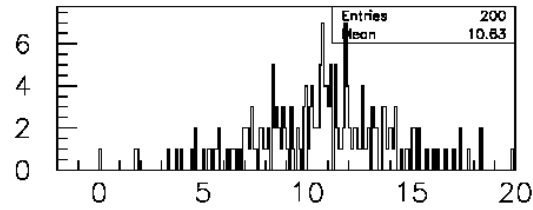


(contd)

0.4 mm gap

2.5 mm gap

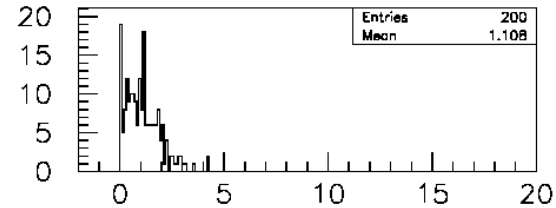
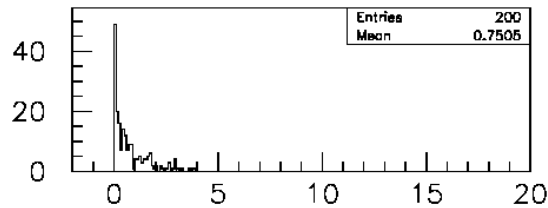
dx = 0



E Dep in pixel, MeV

E Dep in pixel, MeV

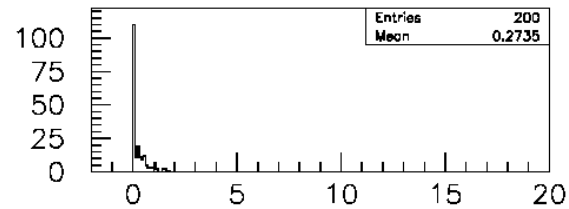
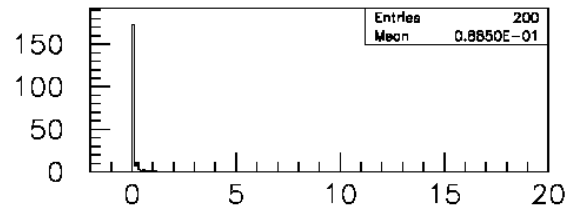
+ 1 pixel



E Dep in pixel, MeV

E Dep in pixel, MeV

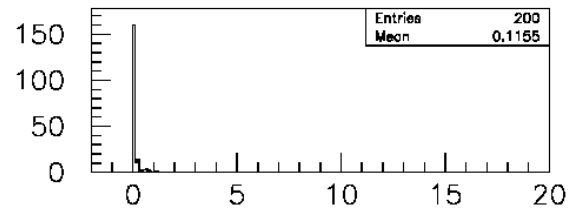
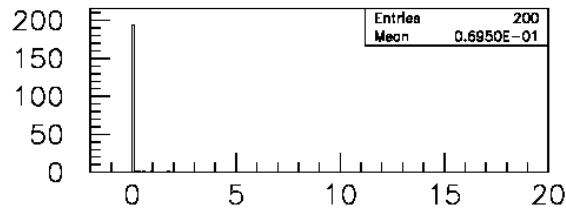
+ 2 pixels



E Dep in pixel, MeV

E Dep in pixel, MeV

+ 3 pixels



E Dep in pixel, MeV

E Dep in pixel, MeV

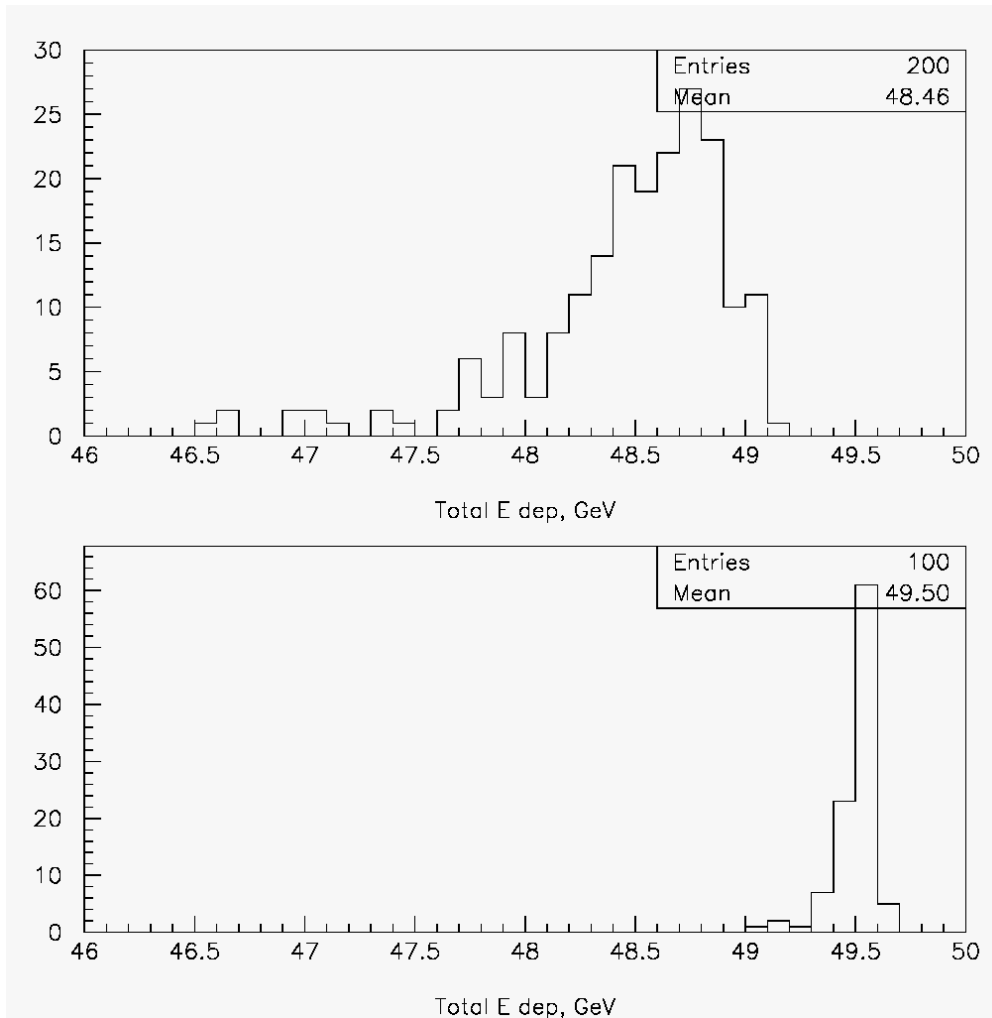
Alternative Sampling Configurations

50 GeV electrons

SD: $30 \times \frac{2}{3} X_0$

SD vB: $20 \times \frac{2}{3} X_0 + 10 \times \frac{4}{3} X_0$

- better containment
- poorer sampling



Global simulation studies needed

- Transverse segmentation and effective Moliere radius
 - EFA jet reconstruction, dummy
 - Tau and μ reconstruction
 - Bhabha acolinearity
- Longitudinal configuration
 - Number of layers ($\approx 1M\$ / \text{layer}$)
 - vs EM resolution (not now limiting jet resolution)
 - vs pattern recognition:
 - Recognize hadronic showers
 - Track MIPs
 - EM shower containment
- Background overlays _ timing requirement

“Technical” simulations planned/in progress

- Geant4 vs EGS4
 - Confirm basic description for Si/W
 - B field on/off
 - Compare with data (e.g. OPAL luminometer)
- Dynamic range
- Distribution of hit occupancy in a detector wafer for jets
- SPICE: S/N, crosstalk, timing, etc.

Status and Plans

- “Current” year
 - Specify silicon detectors for technical prototype studies
 - out for bids
 - Qualify detectors; B field test
 - Design and fab. initial RO chip for technical prototype studies
 - Readout limited fraction of a wafer (\$)
 - Bump bonding; finalize thermal plans
 - Begin tungsten specifications/bids
- Next year
 - Order next round of detectors and RO chips
 - Design and begin fab. of prototype module for beam test
 - Full-depth, 1-2 wafer wide ECal module
- Next-next year:
 - 3rd round of detectors and RO chips ?
 - Begin test beam studies (2005-ish)