

Lab 4: Counters and Registers

4.1 Goals of this Lab

You will build a counter based on component flip-flops, then explore in detail the properties of a IC counter and an IC shift register.

4.2 Asynchronous Ripple Counter

Use flip-flops of the 7476A IC to build the 4-bit asynchronous binary counter shown in Fig. 1. The 7476A is a dual unit, so that there are two flip-flops per IC. Also recall that the 7476A is a J-K type flip-flop. This “A” version of the 7476 latches on negative-going (“negative edge”) clock pulses, rather than positive edges for the non-A version. We wish to use “toggle” mode, with J and K both held high, as you explored in Lab 3. As before, the unused $\overline{\text{CLR}}$ and $\overline{\text{PRE}}$ inputs must be held high.

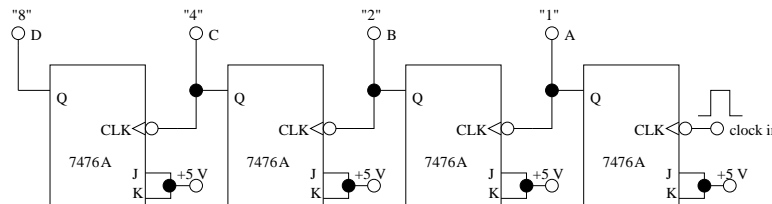


Figure 1: 4-bit counter based on 7476A J-K flip-flops.

4.2.1

Verify the waveforms of Fig. 2. Use an oscilloscope with two inputs: the input clock and the output being studied. You will probably find it easiest to trigger on the clock. Why do we use the negative-edge triggered 7476A, rather than the positive-edge triggered 7476, for this application?

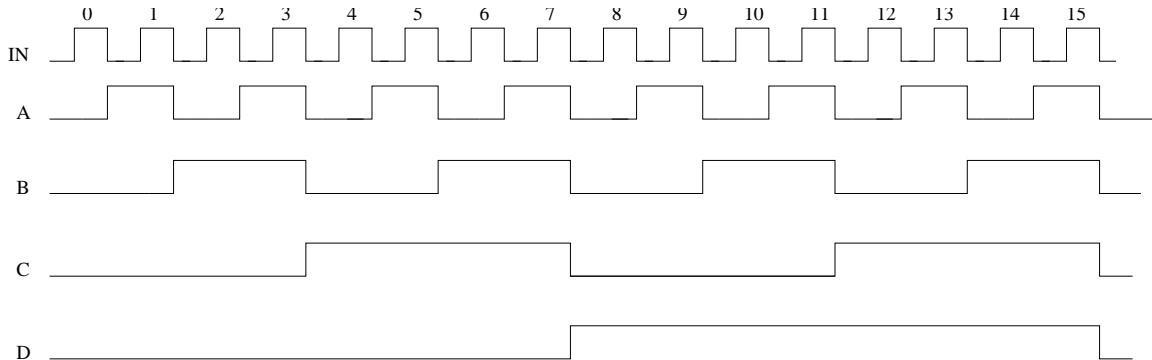


Figure 2: Waveforms associated with the 4-bit counter

4.2.2

How high does your counter count? Does it need to be cleared in normal operation?

4.2.3

The flip-flops can be also wired to count down, rather than up. This is shown in Fig. 3. Build this circuit and verify that it is indeed a down counter. What simple gating scheme could be used to switch between up and down counting modes using a single logic level?

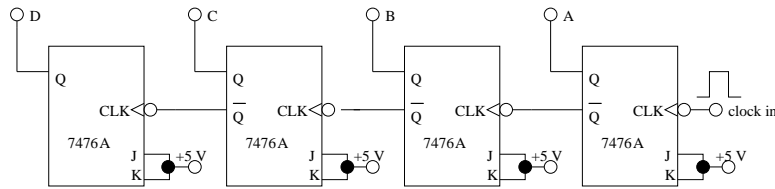


Figure 3: The count down version of the 7476 counter.

4.3 BCD Counter Properties

We have used the 7490 BCD counter previously this term. We wish to explore some of its additional features.

4.3.1

Construct and test the divide-by-6 circuit shown in Fig. 4. Use the oscilloscope again to study the waveforms. Record these. How does it work? How would a divide-by-7 be made? Try it.

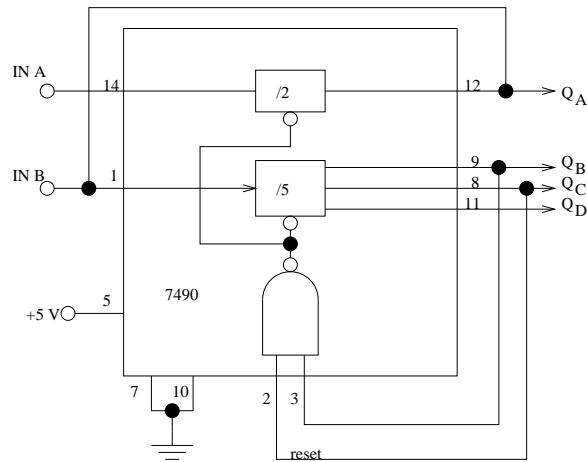


Figure 4: Divide-by-6 circuit based on the 7490 IC.

4.3.2

Internally, the 7490 consists of divide-by-2 and divide-by-5 counters. Hence, a divide-by-10 can be made using a different method than the previous section, in this case resulting in a symmetrical square wave. Connect Q_D to Input A, and use Input B as the input. Record the waveforms and verify the circuit's function.

4.4 Shift Register

The 74195 IC is a 4-bit shift register. Its data sheet is attached. The (serial) input flip-flop has J and \bar{K} inputs. While the SHIFT/LOAD input is held low, parallel data is loaded into inputs A, B, C, and D, and serial shifting is disabled. Then the next clock transition latches the loaded parallel data so that it appears at outputs Q_A , Q_B , Q_C , and Q_D . When the SHIFT/LOAD input goes high, the parallel inputs are disabled and the clock shifts the data through the register serially.

4.4.1

Try parallel loading of various bits and shifting them with clock pulses. Tabulate the inputs and outputs.

4.4.2

Connect the “twisted ring” counter of Fig. 5. Its counting sequence is given in the table below. How does it count? How might it be used?

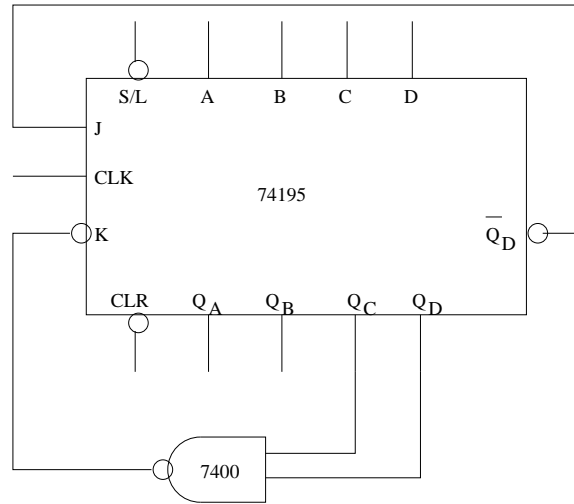


Figure 5: Twisted ring counter.

Table 1: Twisted ring counter count sequence.

Q_A	Q_B	Q_C	Q_D
0	0	0	0
1	0	0	0
1	1	0	0
1	1	1	0
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1