

A SILICON/TUNGSTEN ELECTROMAGNETIC CALORIMETER WITH INTEGRATED ELECTRONICS

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We discuss progress and issues relevant to the design of a highly segmented silicon-tungsten electromagnetic calorimeter. Our design features a complete readout chip which is integrated onto each detector wafer, thus reducing the effective channel count by a factor of about 1000. We apply this design to the SD detector of the American LC Physics Group, but some elements could be applicable elsewhere.

1 Introduction

Accurate jet reconstruction with excellent energy resolution, along with outstanding lepton identification, may turn out to be crucial for characterizing new physics processes at a linear collider. The energy flow algorithm¹ would in principle give unprecedented performance for reconstruction of jet and tau final states. Achieving the full potential of EFA implies the separation and measurement of charged and neutral energy depositions in the calorimeter. Hence, the electromagnetic calorimeter (ECal) should be dense and highly segmented. An attractive possibility is a sampling silicon-tungsten device. Tungsten has a small Molière radius (9 mm) and the silicon can provide practically any transverse segmentation. Hence, one has the possibility of providing a high-quality image of all energy depositions, with the electromagnetic showers confined to small radii. An important application would be the efficient separation of photons and minimum ionizing particles (MIPs) in a jet.

Here, we propose a possible solution for a key technical challenge posed by such a detector, namely the large number of detector elements to be read out, and offer some strategies to minimize cost and improve performance.

2 Silicon and Readout Configuration

The initial SD design concept² calls for an ECal with 30 longitudinal layers each of tungsten and silicon. The tungsten layers have thickness $t_W = 2.5$ mm ($\approx 0.7X_0$). The interleaved readout layers are also set to $t_g = 2.5$ mm thickness. This readout gap t_g must be kept as small as possible in order to preserve the effective Molière radius of the device. With this sampling, the area of silicon for the ECal is roughly 12×10^6 cm². While we expect to further optimize performance against silicon area, it is clear that the cost of the silicon detectors will drive the ECal cost. With a simple and efficient detector design, current trends indicate that we should expect a cost of roughly \$2 per cm² by the time detectors are purchased in large quantity.

The transverse segmentation of the silicon is set to 5 mm \times 5 mm in the initial SD design. This implies 50 million detector pixels to be read out. In our design, we plan to effectively reduce this number by a factor ≈ 1000 . We believe this makes the silicon-tungsten design quite feasible. In fact, the cost in this design is roughly independent of the transverse segmentation.

We hope to use large silicon wafers, which for now we assume to be of 6 inch diameter. Figure 1 depicts the central region of such a wafer, with hexagonal pixels of size 5 mm shown. Each detector wafer would consist of about 1000 such pixels. Metallization on the wafer, indicated with a few lines in the figure, provides the signal traces from each pixel to an array of bump bonding pads, also included in the silicon metallization step. A single 1000-channel readout chip is later bump bonded to this array. As discussed below, this chip provides full digitization of charge and time for the entire detector wafer. Only ~ 10 external lines are required between the chip and the motherboard – power, the zero-suppressed digital output, and various control lines. These are indicated in the cross-sectional view in Figure 2. The digital output goes to a concentrator chip, of which there is about one per ECal module. The area of the readout chip is presently set to 36 mm², but the design allows flexibility, pending full chip layout and prototyping.

The structure of the silicon detectors should be simple in order to minimize fabrication costs. Hence, we intend to use DC coupled detectors. This choice significantly reduces detector complexity and the number of production steps. The detectors would have two metallization layers separated by an insulating layer of thickness 1 to 3 μ m. One metallization layer defines the electric field for each pixel, while the other layer provides the signal traces.

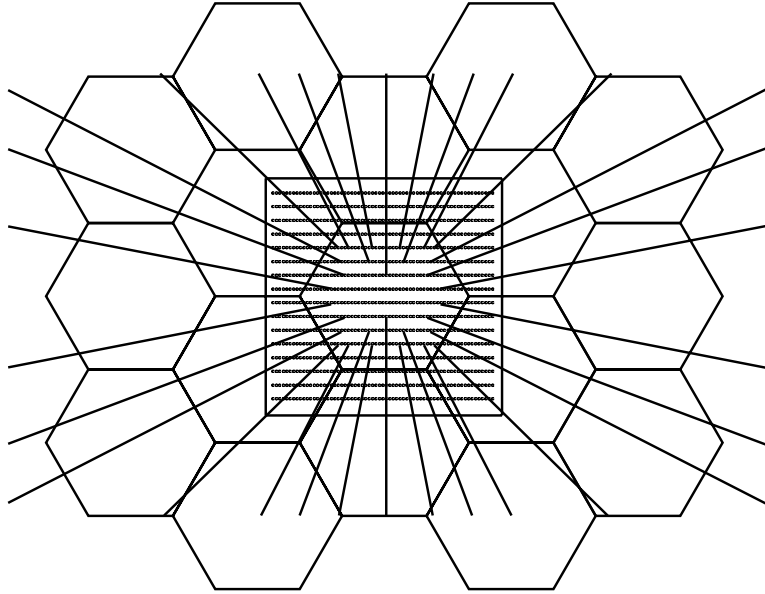


Figure 1: Drawing of the center region of a silicon detector wafer, showing a few detector pixels and the bump bond array for the readout chip. Some representative signal traces are indicated.

3 Readout Electronics Requirements and Challenges

Each ECal pixel must be sensitive to a large dynamic range, from MIPs to Bhabha electrons at the full beam energy. We have evaluated this using an EGS4 simulation which incorporates³ the subtleties in simulating thin silicon sampling layers. We find that the ratio of 500 GeV electron to MIP is 2100 for pixels near shower maximum. (Because of the exponential transverse falloff of shower energy with distance, using smaller pixels does not decrease this significantly.) The requirements for an excellent S/N for MIPs and the large dynamic range leads to a readout element with a two-gain analog stage followed by a multiplexer and 12-bit ADC, effectively providing two overlapping 12-bit ranges. This is indicated in the schematic of one readout channel shown in Figure 3.

We also now plan to include timing for each pixel. This is indicated by the lowest track shown in Figure 3. The idea⁴ is to start a ramp at the beam train start and to measure this ramp at the time of the pixel hit. Our goal is to provide resolution of 10 to 20 ns for a MIP for each pixel, assuming the

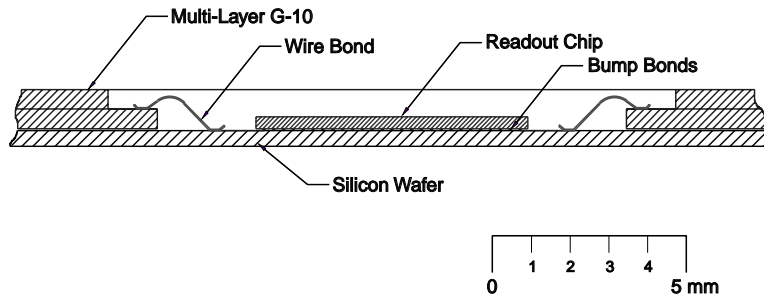


Figure 2: Cross-sectional view in the vicinity of the readout chip.

NLC/JLC bunch structure. This will provide some immunity to backgrounds and allow tagging of multiple physics events within a bunch train.

Because of the embedded electronics, thermal management is critically important in this approach. The best arrangement (for minimizing dead spaces and gaps) would be a fixed temperature heat sink at one edge of the ECal structure, and conduction cooling to this heat sink via a thin copper layer within the readout gap. Thus the maximum thermal path would be about 1 meter. The small accelerator duty cycle at a linear collider plays an important role here, allowing a large average power reduction if power pulsing of the electronics is employed. For NLC (JLC), the duty cycle is only $4(5) \times 10^{-5}$. Therefore, if turn-on transients can be managed, power pulsing should reduce the average front end power by a factor of ≈ 1000 or more. An implication of this technique is that the ECal would not be sensitive to cosmic rays between beam trains. Nevertheless, this approach requires very aggressive control of the average power of the read out chips, representing a fundamental engineering challenge. Our preliminary calculations indicate that we need to keep the average power of the readout chip below 100 mW.

4 Plans

We wish to develop this design in staged prototypes, starting with single chips and wafers to demonstrate the integration approach, leading to construction of a full-depth module for testing in a beam of electrons and hadrons to test simulation codes.

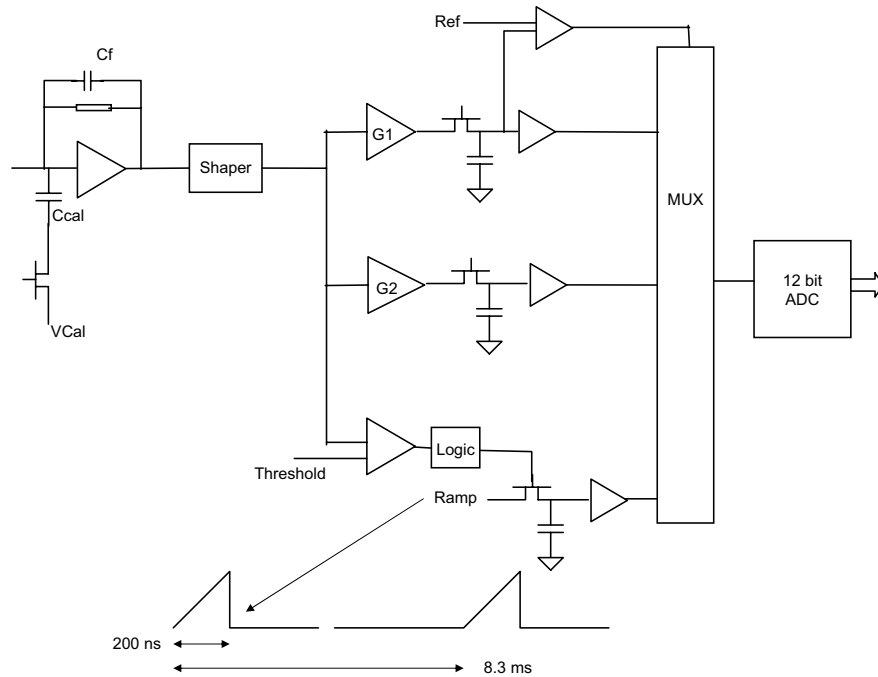


Figure 3: Schematic of one front end electronics channel. We anticipate $C_f \approx 10$ pF and $G_1/G_2 \approx 15$ for a 12-bit ADC. The ramp is used to provide timing. The capacitor $C_{cal} \approx C_f$ is for calibration.

Acknowledgements

This work is supported in part by the US Department of Energy under award DE-FG02-96ER40969 (Oregon) and contract DE-AC03-76SF00098 (SLAC).

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