7 Comparator Circuits

7.1 Simple Comparator

A comparator can be thought of as a fast, high-gain op-amp which is not used with negative feedback. This basic idea is shown in Fig. 38. The comparator has large open-loop gain A. The function of a comparator is to decide which of the two inputs has larger voltage. We have in the limit of very large A

$$v_{\rm out} = A(v_+ - v_-) = \begin{cases} +V_{\rm max} & v_+ > v_- \\ -|V_{\rm min}| & v_+ < v_- \end{cases}$$

where $V_{\rm max}$ and $V_{\rm min}$ are aprroximately the power supply voltages. Therefore, the comparator converts an analog input signal into an output with two possible states. Hence, this can be thought of as a 1-bit analog to digital converter (A/D or ADC). The comparator circuit does not use negative feedback, and so purposefully violates Golden Rule 1. In fact, as we shall see below, comparator circuits often employ *positive* feedback to ensure that nothing intermediate between the two extreme output states is utilized. Finally, without negative feedback, there is no need to do compensation Thus there is more gain at high frequency, meaning faster response. Also, the amplifier can be optimized for speed at the expense of linearity. Comparators, like op-amps, are readily available as integrated circuit chips, such as the model 311 (LM311 or LF311) which we have in lab. Table 9.3 (pages 584-5) of the text lists some of the possibilities on the market.

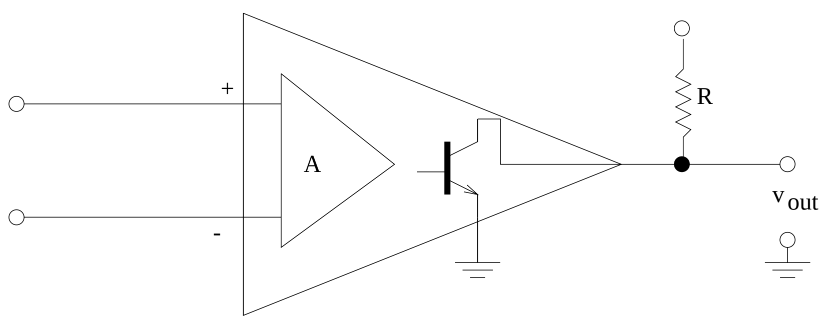

Figure 38: Comparator model.

We have shown explicitly in Fig. 38 the output stage consisting of a transistor with collector connected to the comparator output. This is the *open collector* output, and is typical. It is used in the 311 comparators we use in lab. We are obliged to complete the circuit by providing a "pull-up" resistor R. The transistor emitter is also available as an external connection. It should be connected to whatever is the lower of the two output voltage states we require. This is chosen to be ground in the figure. The high-gain differential amplifier of the comparator has output connected to the base of this transistor. When that is *low* it will, after passing through an inverter, turn the transistor on. In this case, current sill pass through R and to the emitter connection. This current produces a voltage drop across R which pulls the output voltage (very close) to the emitter voltage (ground in our example). Typically $R \approx 1$ kΩ. When the comparator inputs are in the complementary inequality, the transistor is switched off and the output voltage goes to the voltage held by R, which is +5 V in our example. Using outputs of 0 and +5 V are typical, since these voltages correspond (roughly) to the TTL convention of digital electronics.

7.2 Schmitt Trigger

A typical circuit using a comparator is shown in Fig. 39. The output goes to one of its two possible states depending upon whether the input v_- is greater than or less than the "threshold" determined by v_+. Positive feedback is used to help reinforce the chosen output state. In this configuration, called the Schmitt trigger, two thresholds can be set, depending upon which state the output is in. The way this works is illustrated in Fig. 40. V_h and V_l refer to threshold voltages which are set up at the comparator + input by the resistor divider chain. As long as $R_3 \gg R_4$, the output states will still be determined by the pull-up resistor R_4. For the circuit in the figure, these states are 0 and +5 V. The resistor divider, then sets V_+ at different values, depending upon which state the ouput is in. Whether the connection to $+V_1$ and R_1 is required or not depends upon whether a positive threshold is required when $V_{\text{out}} = 0$.

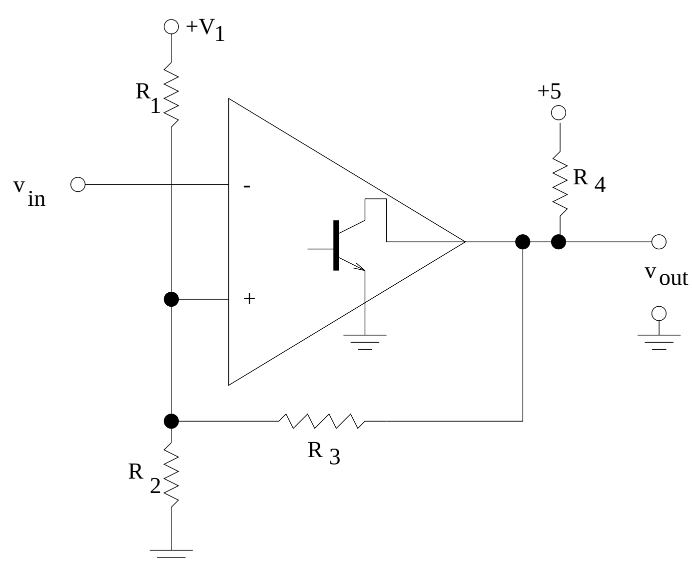

Figure 39: Schmitt trigger.

Referring to Fig. 40, we start with $V_{\text{in}} = V_- < V_+$. The output is in the +5 V state. In this case the threshold produced by the voltage divider, V_h, is the larger value due to the contribution of V_{out}. When the input crosses the threshold, the output changes to the other state, 0 V. The divider then gives a lower threshold V_l. Having two thresholds provides comparator stability and noise immunity. Any noise which is $<< (V_h - V_l)$ will not affect the operation of the comparator.

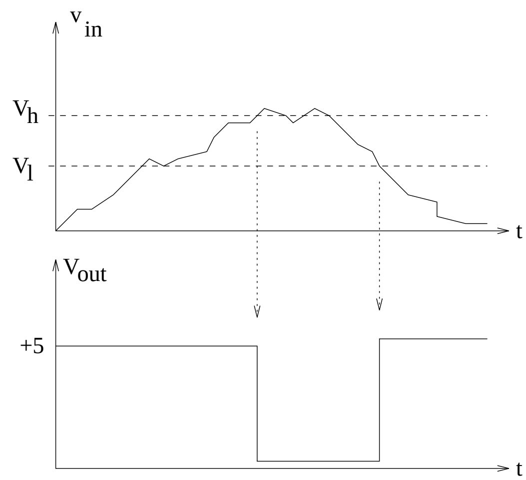

Figure 40: Examples of Schmitt trigger signals versus time. Top: $v_{\rm in}$; the dashed lines indicate the two thresholds set up at the + input of the comparator. Bottom: $v_{\rm out}$.

Note that the resistor R_1 is not necessary if $V_l = 0$. Also, a negative threshold could be set in two ways. The resistor chain forming the threshold could be connected to negative voltage, rather than ground, or the emitter of the output transistor could be connected to negative voltage, thus producing an output with low state at this negative voltage.

7.3 RC Relaxation Oscillator

The circuit of Fig. 41 uses both positive and negative feedback. It is called an RC relaxation oscillator. Note that the positive feedback is a Schmitt configuration. So we expect to have two thresholds. The output voltages are set up to be either +5 V (pull up) or −5 V (emitter connection). Analysis of the voltage divider reveals that the corresponding two threshold at V_+ will be ±1 V. When the output is +5 V, the capacitor C is charged up through the resistor R. The RC part of the circuit is shown in Fig. 42. As we found in class, the voltage across the capacitor, and hence the − input to the comparator, is given (after applying initial conditions) by

$$V_c(t) = V_0 - \frac{3V_0}{2} e^{(t_1 - t)/RC}$$

where t_1 is the time at which the comparator output is first at $V_0 = +5$ V. Hence, the charge up curve will eventually cross the +1 V threshold, forcing the comparator to the −5 V state, and thereby starting a ramp-down of the capacitor voltage given by

$$V_c(t) = -V_0 + \frac{3V_0}{2} e^{(t_2 - t)/RC}$$

where t_2 is the time at which the output switched to −5 V. This ramp down will cross the −1 V threshold, and the whole process will therefore repeat indefinitely. The output will be a square wave, whereas V_c resembles a triangle wave. This is a common technique for building an oscillator.

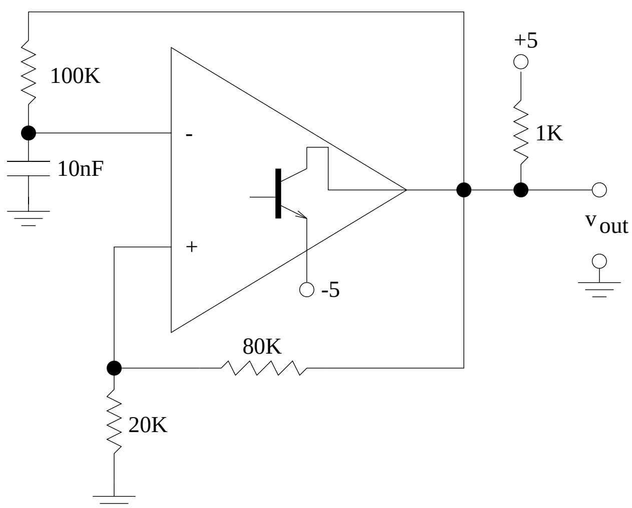

Figure 41: RC relaxation oscillator.

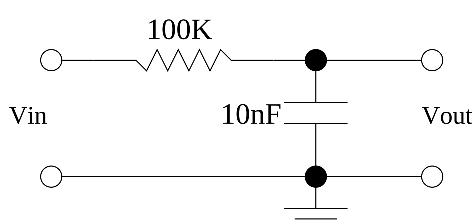

Figure 42: RC circuit with V_{in} from the comparator output and V_{out} going to the $-$ comparator input of previous figure.