

# Lab 5: Op Amps II and Introduction to Phase-Locked Loops

## 5.1 Goals of this Lab

Further exploration of operational amplifier characteristics and associated feedback networks. In the second part, a different type of feedback loop is utilized in a phase-locked loop circuit.

The connections for the model 741 or 411 integrated circuit op-amps used in our labs are shown below in Fig. 1.

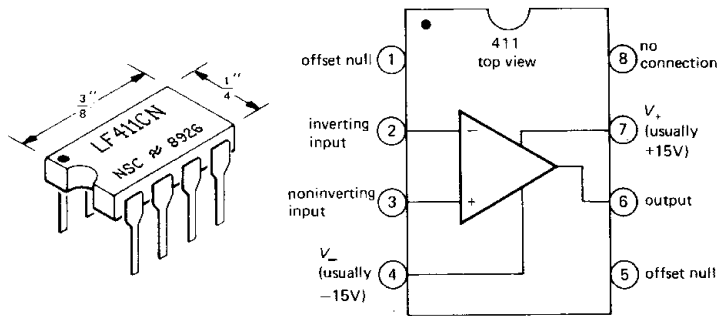


Figure 1: 8-pin DIP package connections for 741 or 411 op-amps.

## 5.2 Integrator

Construct the integrator/low-pass filter circuit shown in Fig. 2. Start with a 741 op-amp. Use a large ( $\sim 0.2$  to  $1 \mu\text{F}$ ) unpolarized capacitor for  $C$  and let  $R_i = 100 \text{ k}\Omega$ .

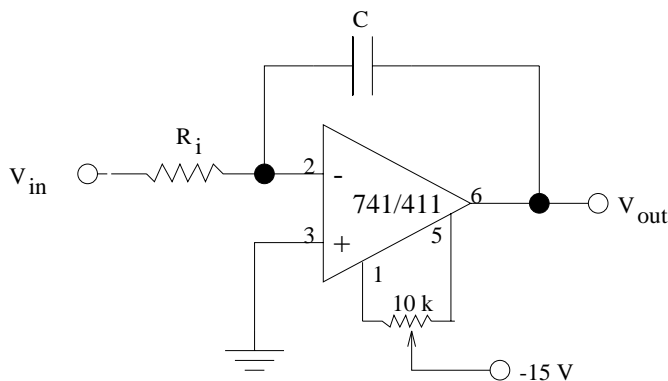


Figure 2: Active integrator.

### 5.2.1

We begin by studying op-amp drifting. Connect the input to ground. While looking at the output with the oscilloscope, initialize the integrator by shorting the capacitor by momentarily putting a  $1 \text{ k}\Omega$  resistor across it. After removing the resistor you will probably observe

the output level drifting. Even if the offset voltage has been carefully zeroed (using the offset balance control via pins 1 and 5), the output will drift due to offset currents. Note the rate of drift in volts per second. Try adjusting the offset voltage balance to see if this can alter the rate of drift.

### 5.2.2

Now replace the 741 with a 411 op-amp. The 411 has JFET inputs, with huge input impedance. The rate of output drift should improve. If the drift is still noticeable, try placing a large ( $\sim 10\text{ M}\Omega$ ) resistor in parallel with  $C$ . Continue with the 411 for the remaining exercises.

### 5.2.3

Input a small DC voltage (using, for example, the offset control of the function generator). Try a few values of  $R_i$  and  $C$  to verify that the output ramp rate is indeed controlled by the product  $R_i C$ .

### 5.2.4

Input a variety of waveforms and draw the input and output. Is this a good integrator? Being sure not to drive the op-amp into saturation, you can use the scope AC input if offset drift continues to be a problem. Vary the frequency of an input sine wave and compare the ratio of output to input amplitudes over a wide frequency range.

## 5.3 Differentiator

Construct the circuit shown in Fig. 3. The role of the  $100\text{ pF}$  capacitor has to do with roll-off stability (see text page 224) and should otherwise be ignorable. Input a sine wave of about  $100\text{ Hz}$  and vary its gain. Is the gain linear with frequency as would be expected for a true differentiator? If the same  $R = 10\text{ k}\Omega$  and  $C = 0.1\mu\text{F}$  were used for a passive differentiator, at about what frequency would it fail? How does that compare with the op-amp version?

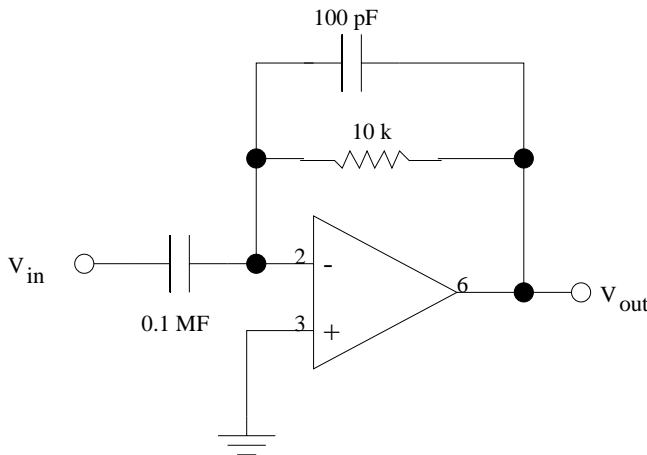


Figure 3: Active differentiator.

### 5.3.1

Input a triangle wave. Note the square-wave output, as expected. Is the square wave perfectly sharp? How might the high-frequency response be improved by modifying the circuit? Try it.

# Introduction to Phase-Locked Loops

The phase-locked loop (PLL) circuit has an enormous number of important applications, including signal (FM) modulation/demodulation, synchronization and replication of weak signals (*e.g.* the “lock-in amplifier”), and frequency multiplication and synthesis. Here, we hope to set up a PLL circuit and to gain some intuition for PLL operation. We will do this with a circuit which uses the PLL as a frequency multiplier. To begin, our input will be at about 60 Hz. Generating multiples of the 60 Hz line frequency is commonly used for noise reduction (due to AC power interference) and other techniques.

Schematically, the PLL circuit looks like that shown in Fig. 4.

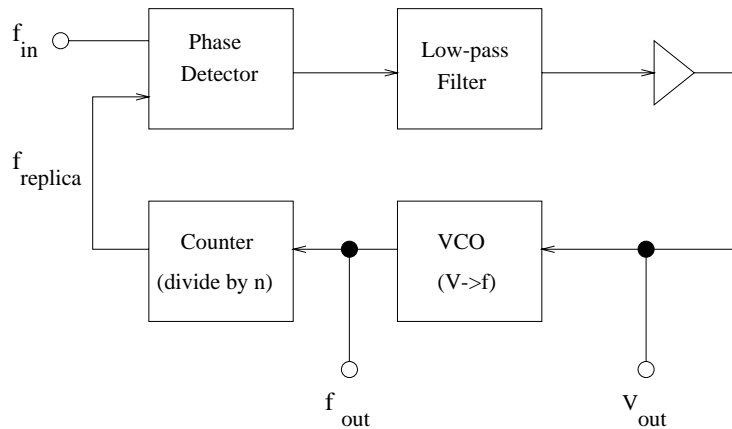


Figure 4: PLL schematic with frequency multiplication.

## 5.4 Frequency Multiplier

The circuit of Fig. 5 is a realization of the general scheme of Fig. 4. Each 4046 PLL chip includes phase detectors (2 types) and a VCO. (A VCO, or voltage-controlled oscillator, is a device which produces an output square wave for which the frequency is proportional to an input voltage.) So, although it is shown functionally as two blocks in the figure, both blocks are on the same IC. See the attached data sheets for more detail and pin assignments. (The 4046 includes an XOR gate phase detector (Type I) output at pin 2 and a state machine phase detector (Type II) at pin 13. We will be using the Type II.)

The 4040 is a 12-stage ripple counter. We will use this to provide the *divide-by-n* function. We will set this up initially with the output taken at  $Q_{10}$ , as shown, which represents a divide by  $n = 2^{10} = 1024$ . That is, for every  $2^{10}$  input pulses, the counter produces one output pulse at pin  $Q_{10}$ .

### 5.4.1

Construct the circuit of Fig. 5. Use the function generator to provide a 60 Hz square wave input with high level (logical TRUE) of 4–5 V and low level (logical FALSE) of 0–1 V. Using the oscilloscope, compare the input and your PLL replica which is input at pin 3 of the 4046. How long does it take the PLL to achieve a stable replica? When this occurs, the PLL is “locked” and the LED should turn on. Do the two signals,  $f_{in}$  and its replica, have the same frequency and phase?

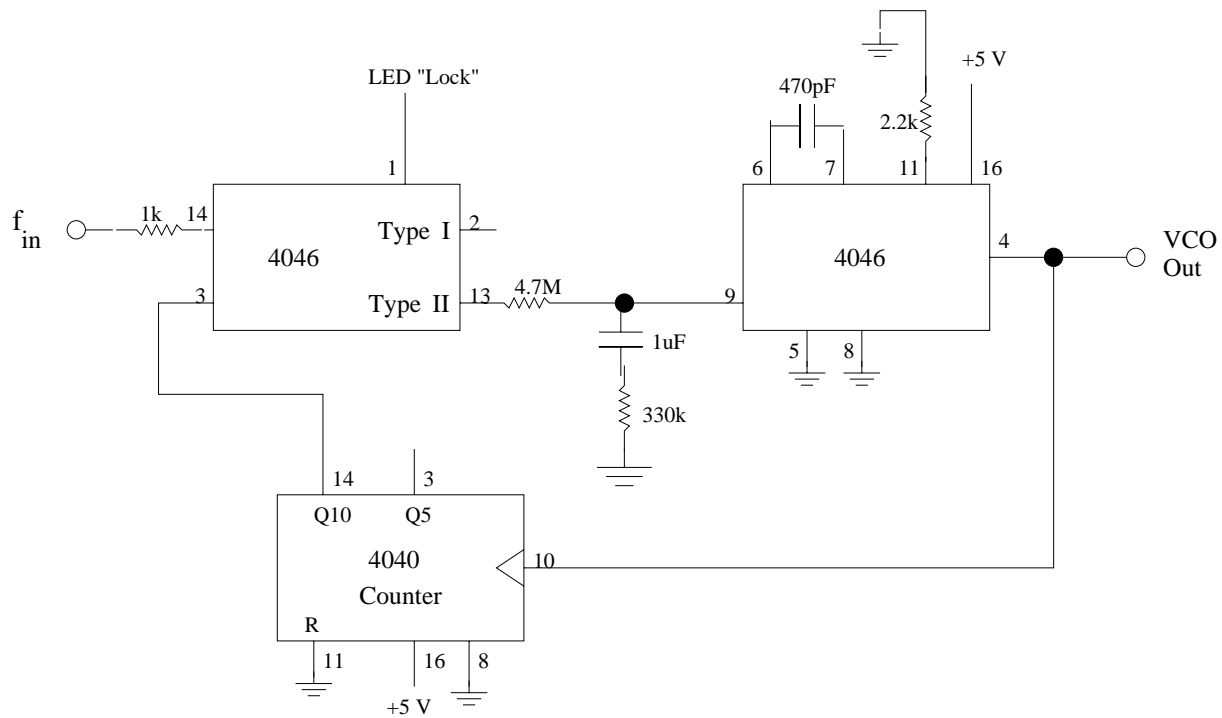


Figure 5: PLL circuit.

#### 5.4.2

Slowly change the frequency of the input. Does the replica follow it? Try abruptly changing the input frequency. How long does it take before the PLL locks again? This can be altered by changing the damping resistor: Change the 330k resistor to 33k and measure (approximately) the change in time to lock. Change it back when you are done.

#### 5.4.3

Measure the frequency at the output of the VCO using the oscilloscope. Is it what you expected?

### 5.5 Expanded Lock Range

Take the replica signal from the  $Q_5$  output, rather than  $Q_{10}$  of the 4040 counter, so that now  $n = 2^5 = 32$ . In order to maintain constant *loop gain*, the damping resistor (330k) must provide increased attenuation by the same factor as the ratio of frequencies. Hence, change it to 10k. With this configuration, your PLL should now be able to achieve lock over a much wider range of input frequency. Measure this range. Would this be sufficient to demodulate audio signals for FM radio? (Recall that the audio range is roughly 20 Hz to 20 kHz.)